# Study on Architectures System for Chip Platforms Using Dynamic Scan

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*Abstract – As the combination, size, and intricacy of the chips proceeds, to scale, the trouble in giving sufficient cooling may either add massive expense or breaking point the usefulness of the registering frameworks which utilize those coordinated circuits. As innovation hubs downsize to 16nm, there is no huge expansion in unique force dissemination. Anyway the static or spillage power increments drastically or surpasses the unique force levels past 65nm innovation hub and arriving at disturbing levels at 28nm innovation hub. This requires viable methods to control both dynamic and static force utilization. Dependability is another vital worry in present day incorporated circuit plan which is normally tended to by the plan for testability models on the chip. Yet, this plan for testability models is in direct clash with the low force objectives. In this postulation different ways to deal with limit cut off, unique force and spillage power scattering at a stage wide level is researched within the sight of a viable plan for test design. A tale strategy for test is proposed which tends to the double objectives of compelling test and diminished force utilization.*

*Keywords – Architectures, Chip Platforms*

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## INTRODUCTION

Low force procedures are required as the mix, size, and intricacy of the chips keeps on scaling. (Moore 2012). The expenses of cooling a chip to forestall chip breakdown in view of warm out of control adds massive expenses or restricts the usefulness of the figuring frameworks which utilize those coordinated circuits. As innovation hubs downsize to 16nm, there is no huge increment (Borkar 2013) in unique force scattering. Anyway the static or spillage power increments significantly or surpasses the unique force levels past 65nm innovation hub and arrives at disturbing levels at 28nm innovation hub ( Shin et al. 2015). This requires compelling strategies to control both dynamic and static force utilization. In this proposal different ways to deal with streamline short out, dynamic and spillage power dispersal at stage wide level is introduced. This proposition tries to inspect the effect of the force network versus the plan for testability grid and the different compromises thereof. The effect of these strategies and resulting compromise choices are concentrated with regards to the cutting edge best in class stage based coordinated circuit plan. It likewise proposes certain key strategies that fill in as powerful compromises in this examination network.

## The boundary scan design

Limit check is a DFT method that is acquired from printed circuit board testing utilizing a standard chip-board test interface. That equivalent strategy and procedure is presently used to empower network check across numerous centers on a SoC. These centers are regularly sourced from different innovation merchants (Mohammad et al. 2009). The Institute of Electrical and Electronics Engineers (IEEE) had set up the business standard for this test interface. The standard known as the IEEE Standard Test Access Port and Boundary Scan Architecture (IEEE Std 1149.1) is regularly alluded to as JTAG. JTAG represents Joint Test Action Group, the gathering that started the normalization of this test interface. Figure 2.3 shows the 1149.1, limit check that empowers chip-level testing by giving direct admittance to the info and yield stack of the coordinated circuits on a SoC. Limit filter changes the I/O hardware of individual centers and adds control rationale so the info and yield stack of each limit examine center can be joined to frame a chip-level sequential output chain (Goh et al. 2015). The limit filter method utilizes the sequential output chain to get to the I/O ports of centers on a SoC. Since the sweep chain is made out of the info and yield stack of centers.
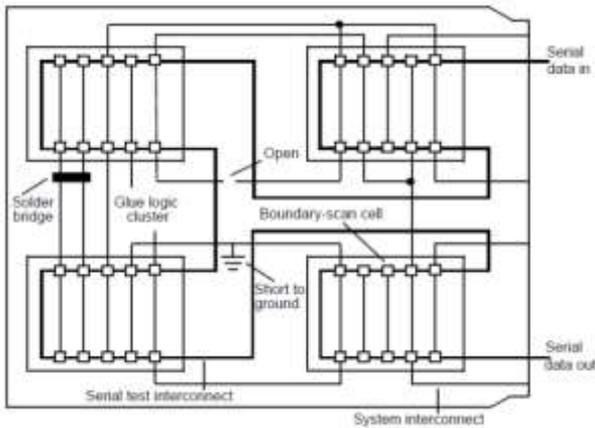
**Figure 1.1 IEEE Std. 1149.1**

In the event that center test methods (inside check) are joined with limit examine a viable testability at both the center and SoC level can be architected. Figure 2.3 portrays a basic SoC with a few limit examine centers and delineates a portion of the disappointments that limit sweep can distinguish.

The centers essential information sources and yields are open on the SoC board for applying and testing information. Limit filter upholds many of the accompanying chip-level test capacities. It empowers recognizing flaws in the interconnect wiring on a SoC for shorts, opens, and spanning issues by testing the bunches of non-limit examine rationale. It distinguishes the absent, bewildered, or wrongly chose segments. It likewise empowers a specific measure of individual center testing on a SoC. In spite of the fact that limit check tends to SoC-test issues, it doesn't straightforwardly address center level testability.

## LITERATURE REVIEW

Low-power structures remembering versatility presents a test to current framework on chip (SoC) and Network on Chip (NoC) Designs ( Bolotin et al. 2014). Particularly, more so if these plans fuse a plan for testability engineering as well. Plan for testability has become the standard in current innovation hubs of IC tapeouts. From a low-power situation, it may appear simple to propose a shut down or force gating or clock gating or DVFS for a specific center to accomplish this. Yet, from a DFT viewpoint this presents an exceptional test as the output chains and their associated tickers must be dynamic for confirmation to occur ( Cecilia et al. 2012 ). Since the force gated or clock gated low-power methodologies can introduce challenges to OnChip investigate particularly in current SoC and NoC which will in general have long test information registers. The drive to low-control configuration ought not effect yield or plan certainty or test certainty (Eric et al. 2015). In SoC configuration, low-power configuration is a key plan issue. Twice as much force is burned-through during testing than during practical activity; the explanation being useful mode inputs are

connected as against test vectors which are genuinely autonomous. Force is disseminated in conventional plan for testability systems in both the successive sweep cells and combinational rationale (Junaid et al. 2016). For the sweep worth to swell down the combinational cone, repetitive exchanging happens which represents around 78% of the all-out test energy (Levitt et al. 2002).

## DESIGN TECHNIQUES

On framework on-chip (SoC) stages number of IP centers run with various clock spaces and most force hungry organization on the SoC is the clock organization. To limit power at framework level, gated clock can be utilized. 10 IP centers which are dynamic utilize the clock and the excess IP centers have their timekeepers incapacitated by utilizing gated clock (Chang 2013). The unique force utilization is straightforwardly relative to the exchanging recurrence, the capacitive burden and the square of the inventory voltage. By limiting the exchanging action of various IP centers on the framework on chip through clock gating, absolute force can be streamlined at high level. Yet, clock gating method can limit power at the expense of expansion in territory. The additional entryways needed for clock gating method may present glitches and clock slant (Shmuel et al. 2014). To limit these glitches and additional clock slant because of clock gating the circuit is overhauled. Additional cradles are included the clock network during clock blend. Utilizing clock gating force can be upgraded at cost of region overhead. There is consistently compromise among region and force plan measurements.

## LOW POWER DESIGN TECHNIQUES

Power reduction techniques fall into two broad categories namely the dynamic power or switching power reduction techniques and the static or leakage power reduction techniques. The issue of power optimization for dynamic power at different levels of design abstraction from circuit to architecture to the system has been well researched in the literature (Michael et al. 2014).

### Dynamic power/switching power/active power

The clock is the sign which flips the most in a circuit. It is additionally, consequently, the wellspring of significant unique force utilization. Clock gating gives a powerful strategy low plan overhead (Marculescu et. al. 2009). The measuring of rationale entryways to adequately lessen the exchanging capacitance is a key plan procedure used to decrease dynamic force just as to accelerate basic ways ( Roy et al. 2010 ). Numerous edge voltages procedure of utilizing double VT semiconductors and allocating low VT semiconductors in basic ways and high VT semiconductors on noncritical ways can help in

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diminishing unique force by 20% and spillage power by half ( Roy et al. 2008). Likewise, basic ways can be appointed high Vdd as against ways on the noncritical ways which are doled out low Vdd. Operand segregation forestalls pointless circuit action by disengagement plan techniques which forestall repetitive calculation. The strategy of diminishing or expanding the recurrence of activity according to require on the fly is called dynamic recurrence scaling ( Sergej et al. 2016 ). In the event that the equivalent is finished with voltage it is called dynamic voltage scaling. Gating the stock utilizing rest semiconductors is another every now and again utilized strategy particularly in customary designs to successfully lessen spillage power utilization.

### Leakage power/standby power

Apart from using dual Vth, proper selection of input vector control can deal up to 35% saving in leakage power. Adding an additional transistor to gate the VSS or VDD line during idle mode effectively saves leakage power. Supply gating using sleep transistors is a very effective method to control leakage on regular structures, like SRAM typically employed in modern SoC architectures extensively (Yaser et al. 2013).

### Power gating (PG)

The power gating technique is a very useful in system on chip platforms because most of the IP cores are not active for schedule activities. By switching off power to IP cores which are not scheduled for current activities, power can be reduced dynamically at top level (Ya-Ting et al. 2016). The dynamic power consumption is directly proportional to square of supply voltage. Supply voltage of IP core has huge impact on top level power consumption. The system on chip platform is built using different IP cores and each IP core may work with different clock domains, multi supply voltages and multi threshold voltages (Yaser et al. 2013). Using power gating techniques unnecessary IP cores can be powered off to minimize power consumption at top level and this may increase area design metric because of extra gates required for this technique. By using power gating stand-by and leakage power can be reduced and this has impact on Iddq testing. In SoC, power gating technique has additional considerations for timing closure implementation. The parameters needed to be considered in power gating technique are power gate size, gate control slew rate, simultaneous switching capacitance and power gate leakage (Goosens et al. 2014). The following methods can be used for the power gating implementation in system on chip platform, fine-grain power gating, coarse-grain power gating, isolation cells, retention registers (Bertozzi et al. 2013).

## DESIGN FOR TESTABILITY TECHNIQUES

In this section various scan design techniques that help us take advantage of a host manufacturing test techniques are discussed. The prominent techniques among them are internal Scan, DFT for System-On-AChip designs and boundary scan designs (Laung et al. 2015).

### Internal Scan

Internal scan is by and far the most widely used DFT technique with the highest scope of fault coverage. The technique reduces the problem of 13 pattern generation by the divide and conquer method. Large sequential designs are divided into fully isolated combinational blocks, typically referred to as full scan design or partially isolated combinational blocks referred to as partial scan designs (Jean et al. 2014). Internal scan in net effect converts the existing sequential elements in the design to support a serial shift capability in addition to their normal functions. The serial shift capability enhances internal node controllability and observability with a minimum of additional I/O pins.

### Scan cells

Figure 2.1 shows a normal flip flop being converted into multiplexed scan flip-flop. This MUX-D scan flip flop can support internal scan in addition to normal operations. Inputs to the multiplexer are the data input of the flip-flop (d) and the scan-input signal (scan_in). The active input of the (Sunnyoul et. al. 2015) multiplexer is controlled by
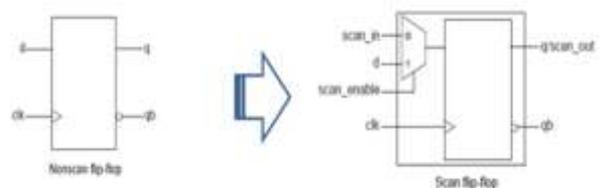


**Figure 1.2 D flip flop with a scanability**

The scan-enable signal. Input pins are added to the cell for the scan in and scan enable signals. One of the data outputs of the flip-flop (q or qb) is used as the 14 scan-output signal (scan_out). The scan_out signal is connected to the scan_in signal of another scan cell to form a serial scan (shift) capability.

### Effect of scan chains on a digital circuit

There are numerous impacts that should be viewed as when adding check hardware to a plan. The plan overhead for testability support builds the region overhead as the output cells are bigger than non-sweep cells. This straightforwardly affects power utilization ( Grammatikakis et al. 2008). The

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presentation of the chip is decreased possibly on account of the greater burden lines and the electrical qualities of the output cells. Worldwide test signals like sweep empower, scan_clk that drive numerous different consecutive components may require buffering to forestall electrical plan rule infringement, similar to hold infringement (Havemann et. al. 2014). This proposition work has utilized the TSMC 28nm innovation library for adding check hardware. By coordinating DFT execution inside union the overhead of sweep hardware dependent on execution, territory, and electrical plan rules is limited. Regularly equality check is done when filter inclusion however as an extra STA, static planning examination, is additionally done on the full sweep netlist. Utilitarian signs connection during STA is of key thought. Output related signals just switch during check mode and are in consistent state during practical mode. That is filter related signs can be aggressors during check mode just and not during practical mode.

## OBJECTIVES OF THE RESEARCH WORK

1.     The scope of the research has been the following. Firstly, to study historically the evolution of IC design and its influence on the present state of IC design process. Secondly, to examine the correlation between low power design techniques and the design for testability (DFT) techniques.

2.     To evaluate the concept of low power in the context of reliability is truly the need of the hour in modern IC design especially at lower geometries below 28nm.

## RESEARCH METHODOLOGY

At a processor level, power advancement can be accomplished at different reflection levels like design, framework and calculation. Yet, even these methods will in general immerse in their proficiency as greater usefulness is incorporated on an IC ( Mezhiba et al. 2015). Innovation level advancement methods is vital. Customarily supply voltage scaling has been endorsed as the most embraced technique for power advancement since it gives critical force investment funds on account of the quadratic connection between exchanging/dynamic capacity to the stock voltage VDD (Friedman et al. 2004). The symptoms of lessening the stockpile voltage are decreased circuit execution. So huge advancements are required in the plan to make up for the presentation decrease brought about by the diminished inventory voltage. The portable business is an exceptionally aggressive industry, where the client requests standout highlights, broadened battery life and extremely low expenses. This requires a drive towards lower innovation hubs and exceptionally undeniable degrees of incorporation at this cycle corners ( Popovich et al. 2008). Yet, these innovation hubs are set apart with second request gadget

impacts and innately higher spillage flows. These high spillage flows present a critical dependability issue as well as an impressive bundling and cooling configuration issues. These issues drive the expenses of the end result fundamentally north ward (Amar et al. 2011).

## SCOPE OF THE PRESENT WORK

Numerous techniques exist in literature to effectively reduce and scale down power consumption on a chip. Reliability is a parallel growing concern as transistor geometries scale down to the now present 14 nanometre (Sinduja et al. 2015). So the objective of the present work has been to study effective implementations of circuit which are both defect aware and at the same time power aware giving a benefit to defect analysis and power consumption numbers simultaneously.

## RESULTS AND DISCUSSION

The recreation results show the effect of force gating on the usefulness of the circuit. The instruments of setting save, reload and plainly found in the underneath waveforms. What's more, value punishments paid in this manner as far as execution. Current circuits are more engaged to time basic than territory basic. The circumstance chart in figure 4.14 subtleties the component of stopping the FSM activity of the SPARC center as a result of the force gating and relevant saving (Context Save) of the states to empower restart of the state (Context Restart) . As laid out the control is kept up by a consistently on center. The consistently on center runs the CS, CR and setting stacking states to empower successful control and forestalling power outages or state defilements.
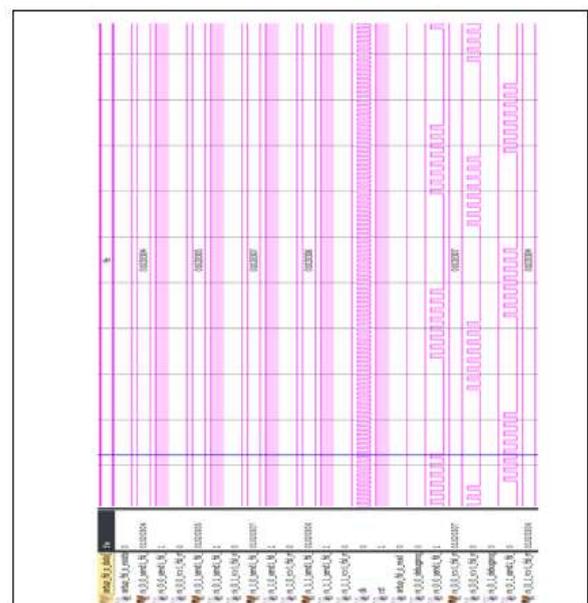


**Figure 1.3 Effect of power gating on the timing of the Circuit**

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## CONCLUSIONS

To improve the unwavering quality of the present multiprocessors, we need to coordinate SoC engineering with both low-power plan and plan for testability which is exceptionally difficult. To upgrade force, territory, and execution and unwavering quality is likened to "loosening the gordion hitch". With dynamic sweep low-power plan for test engineering it is shown that on the Ultras ARC CMP that force utilization can get decreased by a factor of up to 15% while as yet keeping up high unwavering quality of the chip simultaneously acquire a territory advantage of 7%. It likewise empowers simple joining of more up to date macros in particular manner. What's more, powerful sweep is a vital commitment in this field.

## REFERENCES

1.  Bawa and N. A. Touba (2015). "Improving X-tolerant combinational output compaction via input rotation", IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFTS), Amherst, MA, pp. 167-170.

2.  Ashwini Bhore and Gayatri Bhandari (2015). Review on Automatic Test Packet Generation‖, International Journal of Engineering Technology and Computer Research, Volume 3, No 6, pp. 35- 42.

3.  Barnhart, V. Burnkhorst, F. Distler, O. Farnsworth, B. Keller, and B. K¨onemann —OPMISR: The foundation for compressed ATPG vectors‖, Proceedings IEEE International Test Conference, pp. 748- 757.

4.  Barnhart, V. Burnkhorst, F. Distler, O. Farnsworth, B. Keller, and B. K¨onemann: OPMISR: The foundation for compressed ATPG vectors‖, Proceedings IEEE International Test Conference, pp. 748- 757.

5.  Cecilia Metra , Martin Omana,T.M. Mak and Simon Tam (2012). New design for testability approach for clock fault testing‖, IEEE transactions on Computers , Volume: 61 , Issue: 4, pp. 448 – 457.

6.  Eric J. Fluhr . et al. (2015). The 12-Core POWER8™ Processor With 7.6 Tb/s IO bandwidth, integrated voltage regulation, and resonant clocking‖ IEEE Solid-State Circuits Society ,Volume: 50 , Issue: 1, pp. 10 – 23.

7.  H. B. Bakoglu (1990). Circuits, Interconnects, and Packaging for VLSI‖, Reading , Addison-Wesley Publishing Company, MA.

8.  K. Banerjee, S. J. Souri, P. Kapur, and K. C. Saraswat (2001). 3-D ICs: A Novel Chip Design for Improving Deep Submicron Interconnect Performance and Systemson-Chip Integration‖, Proceedings of the IEEE, 89(5), pp. 602- 633.

9.  K. Banerjee, S. J. Souri, P. Kapur, and K. C. Saraswat (2001). 3-D ICs: A Novel Chip Design for Improving Deep Submicron Interconnect Performance and Systemson-Chip Integration‖, Proceedings of the IEEE, 89(5), pp. 602- 633.

10. Michael Richter and Krishnendu Chakrabarty (2014). Optimization of test pin-count, test scheduling, and test access for NoC-based Multicore SoCs‖, IEEE transactions on Computers, Volume: 63 , Issue: 3 , pp. 691 – 702.

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