Journal of Advances and Scholarly Researches in Allied Education
Vol. 16, Issue No. 3, (Special Issue) March-2019, ISSN 2230-7540

Simulation and Analysis of Multilevel Inverters for 3-Phase Motor Speed Control

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Abstract – The relevance of multilevel inverters has been increased since last few decades. These new types of inverters are suitable for high voltage and high power application. However the conventional topologies used in electrified traction system causes power quality issues such as high harmonics distortion, low power factor on ac line due to the nonlinear nature of the load. To address the said issues, this paper presents a topology of 7-level asymmetrical cascaded converter based on the series connection of cascaded module of five levels converter (CM), with H-bridge cell to meet the demand of traction application with improved power factor at minimum harmonics distortion. The proposed topology consists of a single dc source and two dc-link capacitors to obtain the desire level of output with minimum power switches. Harmonics compensation is achieved by providing H-bridge cell and cascaded module with a gating signal at fundamental frequency and high switching frequency respectively. Working principle of proposed topology, mathematical analysis, controlled PWM strategy, stability problem related to dc-link capacitor voltage, possible means of balancing and results has been fully investigated with the help of simulation.

Keywords: Multilevel, THD, Comparison, Sine PWM

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I. INTRODUCTION

Multilevel inverters include an array of power semiconductors and capacitor voltage sources, the output of which generate voltages with stepped waveforms. The term multilevel starts with the three-level inverter introduced by Muhammad, et. al. (2017). By increasing the number of levels in the inverter, the output voltages have more steps that is, a staircase waveform, with reduced harmonic distortions. A multilevel inverter has several advantages over a conventional two-level inverter that uses high switching frequency pulse width modulation (PWM). The main attractive features of a multilevel inverter are (Muhammad, et. al., 2017) :

1) **Low dv/dt stress**: Multilevel inverters not only can generate the output voltages with very low distortion but also can reduce the dv/dt stresses.

2) **Common-mode (CM) voltage**: Multilevel inverters produce smaller CM voltage; therefore, the stress in the bearings of a motor connected to a multilevel motor drive can be reduced.

3) **Input current**: Multilevel inverters can draw input current with low distortion.

4) **Switching frequency**: Multilevel inverters can operate at both fundamental frequency and high switching frequency PWM. It should be noted that lower switching frequency usually means lower switching loss and higher efficiency.

Multilevel inverters do have some disadvantages. One being the requirement of many power semiconductor switches. Also each switch requires a related gate drive circuit. This may cause an increase in overall expenses of the system.

II. MULTILEVEL INVERTER TOPOLOGIES

Multilevel inverters can be mainly divided into three major types:

a) **Cascaded H-bridge multilevel inverters:** These inverters include several H-bridge cells (Full-bridge inverters) connected in series.

b) **Diode-clamped multilevel inverters:** These inverters use clamped diodes and dc capacitors in order to generate ac voltage. This structure is known as neutral-point clamped (NPC) and is widely used in medium voltage, high power drives.

c) **Flying-capacitor multilevel inverter:** In this topology, semiconductor devices are in series and their connecting points are clamped by extra capacitors.

d) **Cascade h-bridge multilevel inverter:** A structure of an m-level cascaded inverter is shown in Fig.1. Each separate dc source (SDCS) is connected to a H bridge inverter. The number of output phase voltage levels, *m*, is given by *m = 2s+ 1* , where s is the number of separate dc sources (Atkar, et. al., 2016). Cascaded inverters have been used for such applications as static var generation, with renewable energy sources, and in battery-based applications. The main advantages and disadvantages can be listed as (Siksha, 2015):-

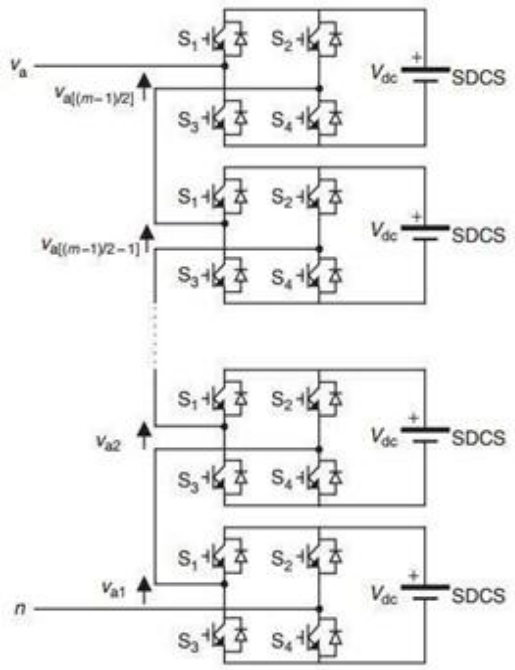

Fig. 1. Structure of a multilevel cascaded H-bridge inverter (Atkar, et. al., 2016)

III. MULTICARRIER PWM TECHNIQUES

The based PWM Techniques for cascade multilevel inverter can be broadly classified into:-phase shifted modulation and level shifted modulation (Lekha, 2013). In to both techniques, for an m level inverter, (m-1) triangular carrier waves are required. And all the carrier waves should have the same frequency and the same peak to peak magnitude.

a) **Phase shifted multicarrier modulation**

In phase shifted PWM (PS-PWM), there is a phase shifted of Φ_{cr} between the adjacent carrier signals. The phase shifted is given by

$$\Phi_r = 360^0/(m\text{-}1)$$

for a three phase inverter, the modulating signals should also be three phase sinusoidal signals with adjustable magnitude and frequency. For this modulation scheme, the frequency modulation index m_f and the amplitude modulation index m_a is given by-

$$m_f = f_{cr}/f_m$$

And

$$m_a = V_{mA}/V_{cr}$$

where f_{cr} and f_m is the frequency of the carrier and the modulating signals respectively and v_{cr} and v_{mA} are the peak amplitudes of the carrier and the modulating signals respectively. The amplitude modulation lies in the range of 0 to 1. The switching frequency of the device can be calculated as $f_{dev} = f_{cr} = f_m \times m_f$. the switching frequency of the inverter can be found from the device switching frequency ass f_{inv}=(m-1) i.e. 4 number of carrier waves of the same

Frequency and having the same peak to peak magnitude as shown in fig 2.

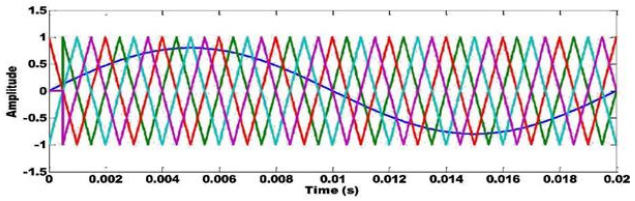

Fig 2. Phase-shifted PWM for five level CHB inverters

b) **level shifted multicarrier modulation**

In level shifted PWM (LS-PWM), the triangular waves are vertically displaced such that the bands occupy are contiguous. The frequency modulation is given by $m_f = f_{cr}/f_m$ and amplitude modulation index is $m_a = v_{ma} / (m\text{-}1)v_{cr,}$ where f_m and f_{cr} are the frequencies of the modulating and carrier waves and v_{ma} and v_{cr} are the peak amplitude of modulating and carrier waves respectively. The amplitude modulation lies in the range of 0 to 1. Depending upon the disposition of the carrier waves, level shifted PWM can be in phase

disposition PWM (IPD – PWM), phase opposition disposition PWM (POD – PWM) and alternate phase opposition disposition PWM (APOD – PWM).

i) **IPD-PWM:-** In this modulation, all the triangular carrier wave are in phase As shown in fig 3.

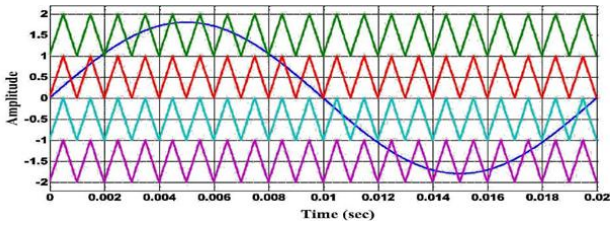

Fig 3. in phase disposition PWM for five level CHB inverter

ii) **POD-PWM:-** The carrier waveforms are in all phase above and below the zero reference value; however there is 180^0 phase shift between the ones above and below zero respectively as shown in fig 4.

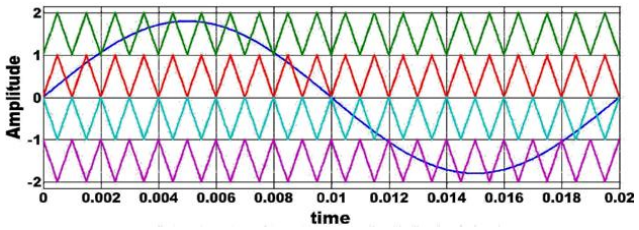

Fig 4. in phase opposition PWM for five level CHB inverter

iii) **APOD-PWM:-** The carrier waves have to be displaced from each other by 180^0 alternately as shown in fig 3.4. In this modulation, the inverter switching frequency and the device switching frequency is given by $f_{inv} = f_{cr}$ and $f_{dev} = f_{cr}/(m-1)$ respectively.

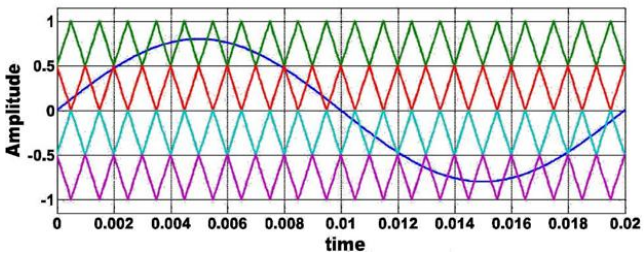

Fig 5. Alternate phase opposition disposition PWM for five level CHB inverter

In LS-PWM, each carrier is associated with the gating signals of NPC converter whereas in PS-PWM, a pair of carriers is associated with each cell of the CHB and FC converters. Because of the phase shifting of the carriers, power is evenly distributed among the cells which results in the smooth operation of CHB and the natural voltage balancing of the FC. Therefore, LS-PWM is mainly used for NPC converter whereas PS-PWM is practically used for CHB and FC converter. Even though IPD-PWM results in low THD as compared to PS-PWM, the small difference in the high frequency content can be filtered out (Khoucha, et. al., 2010).

IV. SIMULATION AND ANALYSIS

Matlab Simulation of Multilevel Inverter control for AC Motor

The usual technique of overcoming such problems in voltage source inverters is to pulse width modulate the input voltage waveforms. Pulse width modulated voltage source inverters are invariably used for AC/DC/AC conversion to provide a variable ac voltages to the induction motor. However, inverter fed induction motor suffers from the presence of significant amount of harmonics which causes undesired motor heating, torque pulsation and electro-magnetic interference. In order to reduce the harmonics, large sized filters are needed, which results in larger size and increased cost of the system. However the advanced achievements in the field of industrial electronics and power electronics made possible to reduce the magnitude of harmonics using multilevel inverter structures, in which the number of output voltage and current waveforms are increased without increasing the size of the filter.

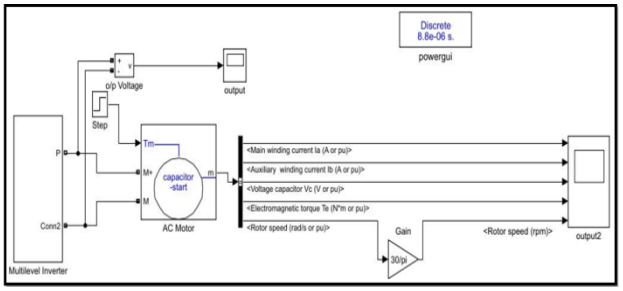

Fig 6- Multilevel Inverter fed AC Motor

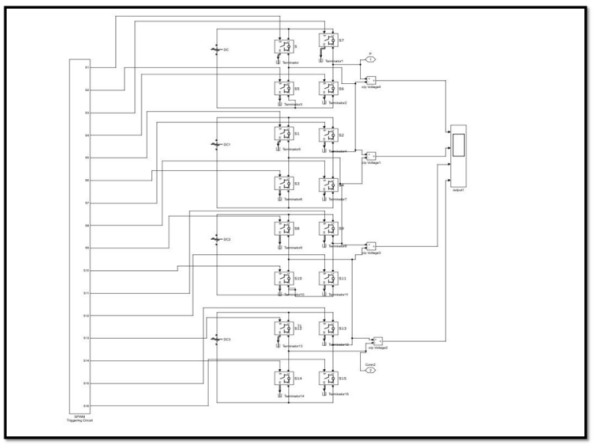

Fig 7- Multilevel Inverter Subsystem

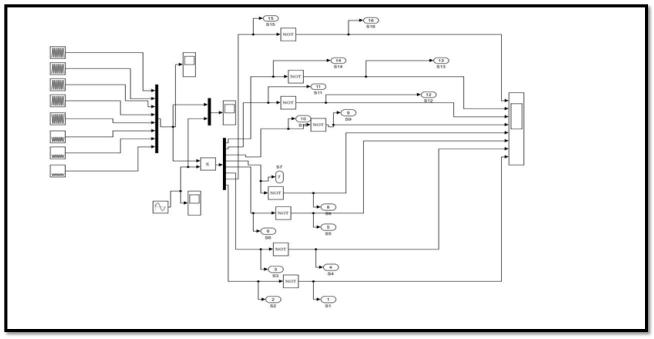

Fig 8- Inverter Triggering Pulse Control subsystem

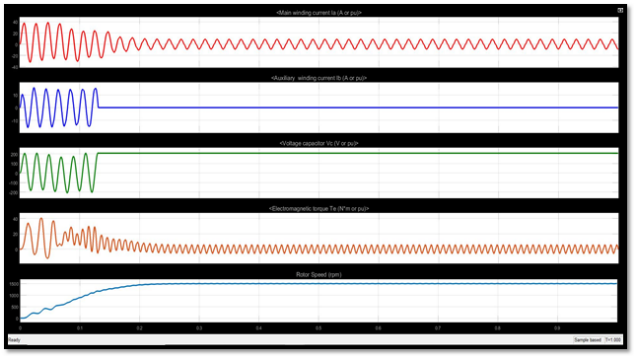

Fig 9- AC Motor Output Control Parameters

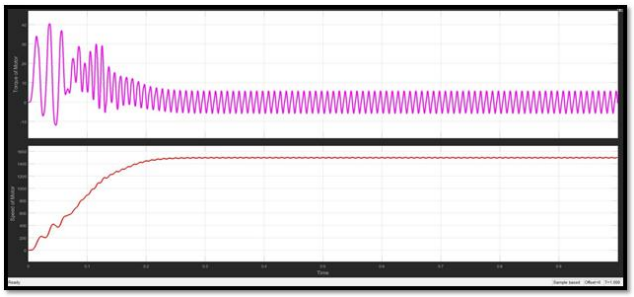

Fig 10- AC Motor Output Torque and Speed Waveform

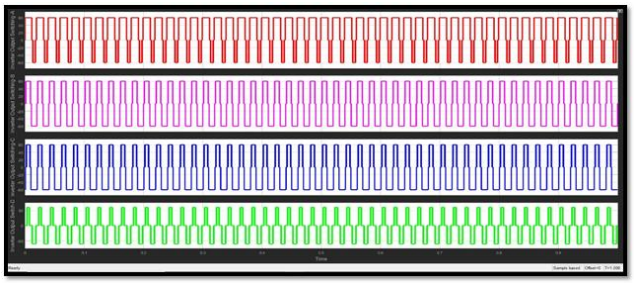

Fig 11- Switching output of Inverter

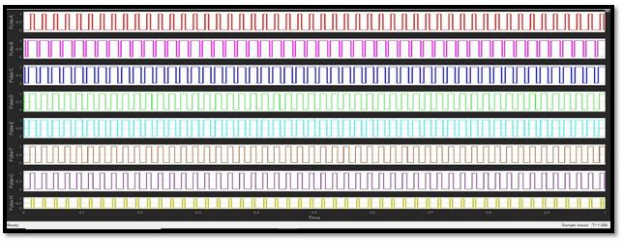

Fig 12- Triggering Pulses for Inverter

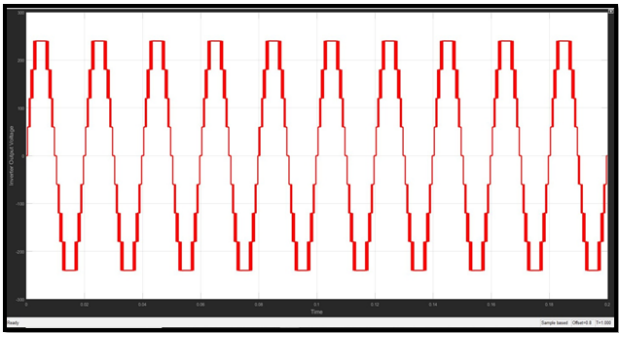

Fig 13- Inverter Output Voltage

Matlab Simulation of Inverter fed BLDC Motor Control

The proposed three-phase MLI fed to the BLDC motor is shown in Fig.14. This model represents modeling three-phase, three-level inverter. The 12-inverter pulses required by the inverter are generated by the discrete three-phase PWM generator. The system operates in open loop at a constant modulation index. The inverter is built with individual IGBTs and diodes. In a three-level voltage-sourced converter (VSC) using ideal switches, the two pairs of pulses sent to each arm could be complementary. For example, for phase A, IGBT1 is complementary of IGBT3 and IGBT2 is complementary of IGBT4.

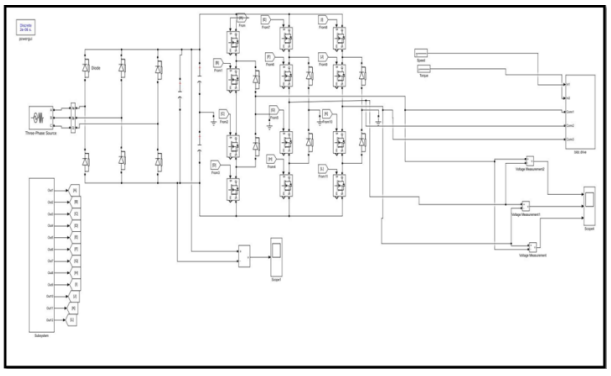

Fig 14- Inverter fed BLDC Motor

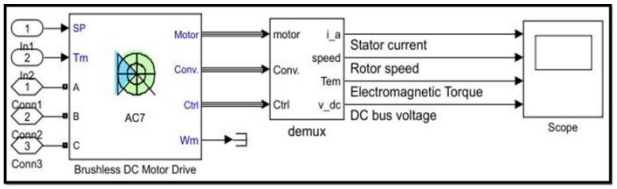

Fig 15- BDLC Motor Subsystem

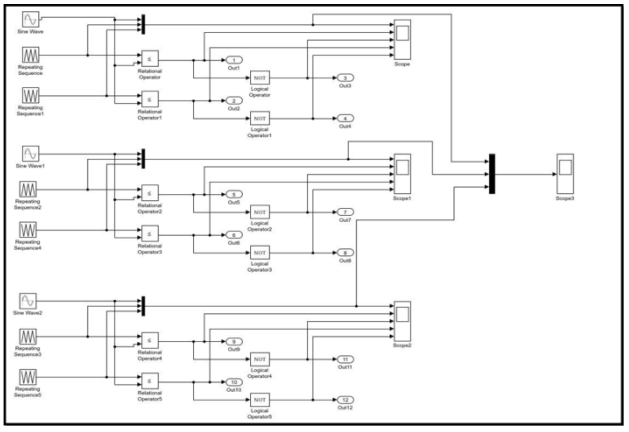

Fig 16- Triggering Pulse Control Subsystem

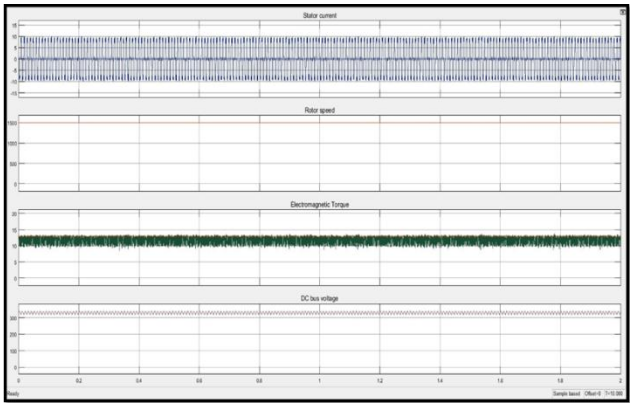

Fig 17- BLDC Motor Output Parameters

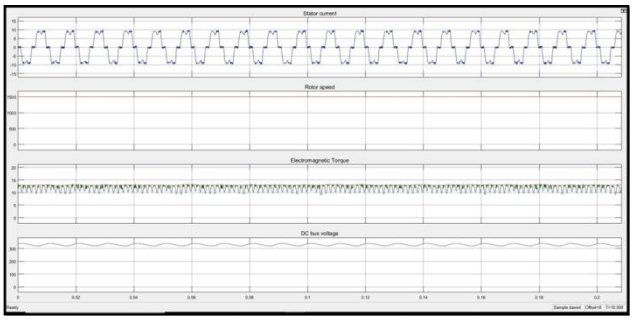

Fig 18- BLDC Motor Zoom scale output

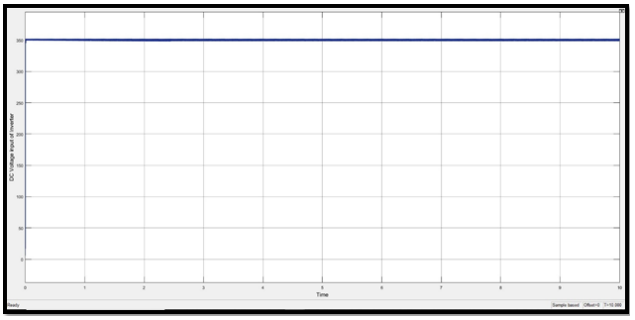

Fig 19- Inverter Input D.C Voltage

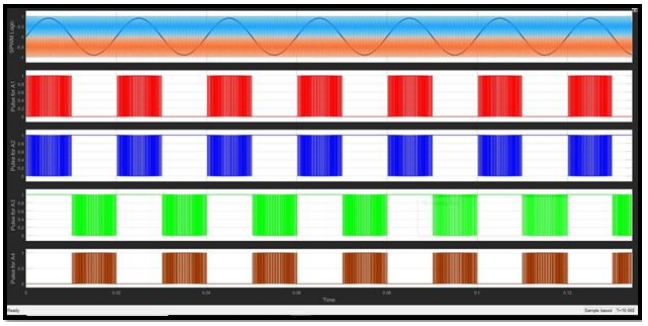

Fig 20- Triggering Pulses for Inverter

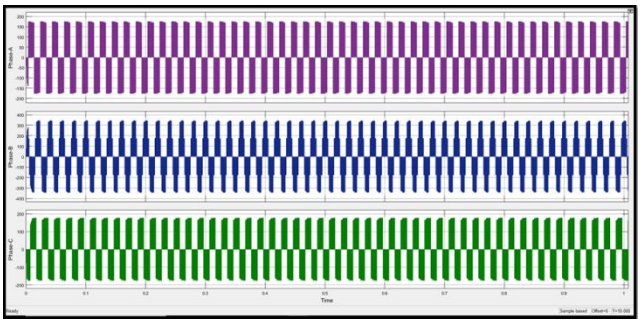

Fig 21- Inverter Output Voltage

V. CONCLUSION

Various Multilevel inverter topologies were studied using simulation results. The three level, seven level cascaded H-bridge inverters were simulated in MATLAB-Simulink environment. Two types of Multicarrier Pulse Width Modulation – Level Shifted Modulation and Phase Shifted Modulation were implemented for the cascaded multilevel inverter. It was found that the cascaded h bridge inverter configuration gave sinusoidal output waveform. This converter system can meet the power or voltage requirement of the traction drive. The cascaded eleven level converter system modeled in this project can be used in traction drive consisting of four induction motors for stepping down the catenary voltage to the rated voltage of the induction motors. The Matlab Simulation of Multilevel inverter for I.M Speed control and BLDC motor speed control is done successfully as shown in the simulation results.

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