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Simulation and Fault Analysis of HVDC Line Protection using C.B.

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Abstract – Recently, studies on HVDC circuit breaker (CB) prototypes have shown successful take a look at results. Nevertheless, effective and reliable solutions relating to massive fault energy during dc fault interruption have not nevertheless been commercialized, and dc current breaking topologies on ways of achieving artificial zero should be somewhat modified. As another, one possible resolution is to mix fault current limiting technologies with dc breaking topologies. In this paper we studied the applying of resistive superconducting fault current limiters (SFCLs) on various sorts of HVDC CB so as to estimate the consequences of combining fault current limiters and conventional dc breakers. For the simulation works, four sorts of dc breaker topologies were modeled, as well as a mechanical CB using black-box arc model, a passive resonance CB (PRCB), an inverse current injection CB, and a hybrid HVDC CB. In addition, a resistive SFCL was simulated and added to the dc breakers to verify its interruption characteristic and distributed energy across HVDC CB. From the simulation results, we have a tendency to found that the utmost fault current, interruption time, and dissipated energy stress on the HVDC CB might be decreased by applying SFCL. In addition, it had been observed that, among four types of HVDC CB, PRCB with SFCL exhibited the best observable enhancement.

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INTRODUCTION

HVDC transmission network is better than HVAC transmission for long transmission system. Due to the significant progress in power electronics technology during the past two decades, the use of High Voltage Direct Current (HVDC) power transmission is becoming more and more attractive. The HVDC system consisting of two or more such HVDC links is called multi grid HVDC system. In order to achieve commercial application of future Multi Terminal HVDC (MTDC) networks, typically considered an optimum solution for renewable energy transmission and power grid inter-connection, the reliability of HVDC systems must be guaranteed. Conventional point-to-point HVDC systems can be sufficiently protected via mechanical circuit breakers located on the AC side, however, a selective coordination protection scheme that isolates faulted lines should be utilized in MTDC to prevent the blackout of the entire grid system. HVDC circuit breakers (HVDC CB) are widely considered a key technology in the implementation of the MTDC system. Generally, fault current interruption can be easily achieved via zero-current crossing. While AC circuit breakers can interrupt a fault current in natural zero current, artificial current zero should be implemented for DC breakers to enable fault current interruption. To fulfill the zero-crossing condition of DC fault current, a forced current reduction method should be utilized, and various type of HVDC CB are summarized in, some of which have revealed prototypes and successful test results. Nevertheless, an effective and reliable solution considering massive fault energy during DC fault interruption is still lacking. Existing DC current breaking topologies focusing solely on methods to achieve artificial current zero should be somewhat modified. As an alternative, one feasible solution is to combine fault current limiting technologies with DC breaking topologies.

In this work, we investigated application studies of resistive SFCL on the various types of HVDC CB in order to estimate the effects of combining fault current limiters and conventional DC breakers. Resistive SFCL have been acknowledged as an effective solution to effectively limit fault current levels by absorbing electrical and thermal energy stresses during fault. In this light, the combined application of SFCL and HVDC CB could be an attractive alternative solution capable of drastically decreasing the dissipated fault energy and improving the performance of HVDC CBs. In order to estimate the performance of combined application of SFCL on HVDC CBs, simulation studies were performed using Matlab/Simulink.

HVDC SYSTEM

General:

Over long distances bulk power transfer can be carried out by a high voltage direct current (HVDC) connection cheaper than by a long distance AC transmission line**. HVDC** transmission can also be used where an AC transmission scheme could not (e.g. through very long cables or across borders where the two AC systems are not synchronized or operating at the same frequency).

The HVDC technology is a high power electronics technology used in electric power systems. It is an efficient and flexible method to transmit large amounts of electric power over long distances by overhead transmission lines or underground/submarine cables.

There are different types of HVDC systems which are:-

Mono-polar HVDC system:

In the mono-polar configuration, two converters are connected by a single pole line and a positive or a negative DC voltage is used. In Fig there is only one Insulated transmission conductor installed and the ground or sea provides the path for the return current**.**

Figure 1 monopole HVDC system

Bipolar HVDC system:

This is the most commonly used configuration of HVDC transmission systems. The bipolar configuration, shown in Fig. Uses two insulated conductors as Positive and negative poles. The two poles can be operated independently if both Neutrals are grounded. The bipolar configuration increases the power transfer capacity. Under normal operation, the currents flowing in both poles are identical and there is no ground current. In case of failure of one pole power transmission can continue in the other pole which increases the reliability. Most overhead line HVDC transmission systems use the bipolar configuration.

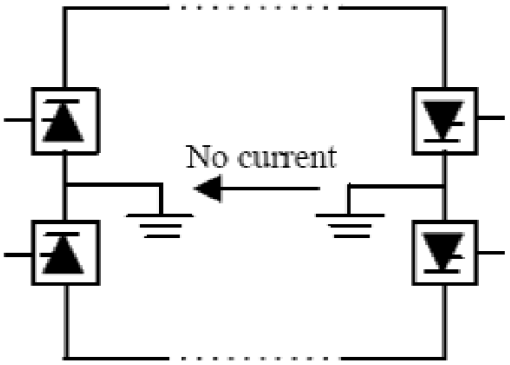

Figure 2 Bipolar HVDC system

Homo-polar HVDC system:

In the homo polar configuration, shown in Fig. Two or more conductors have the negative polarity and can be operated with ground or a metallic return. With two Poles operated in parallel, the homopolar configuration reduces the insulation costs. However, the large earth return current is the major disadvantage.

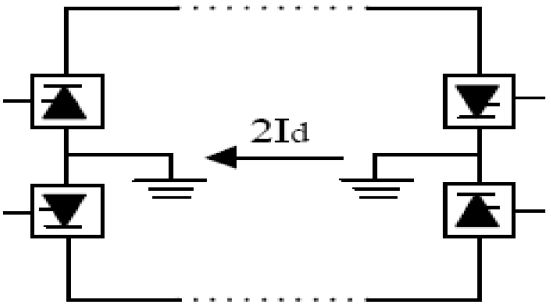

Figure 3homopole HVDC system

Multi-terminal HVDC system:

In the multi terminal configuration, three or more HVDC converter stations are geographically separated and interconnected through transmission lines or cables. The system can be either parallel, where all converter stations are connected to the same voltage as shown in Fig(b). or series multi terminal system, where one or more converter stations are connected in series in one or both poles as shown in Fig. (c). A hybrid multi terminal system contains a combination of parallel and series connections of converter stations.

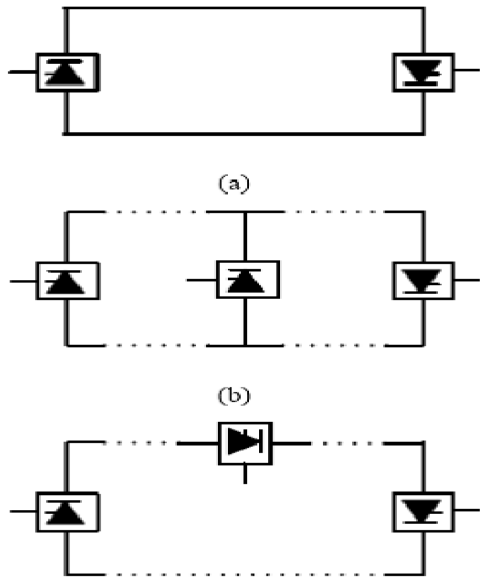

Figure 4 Multi terminal HVDC system

HVDC SYSTEM

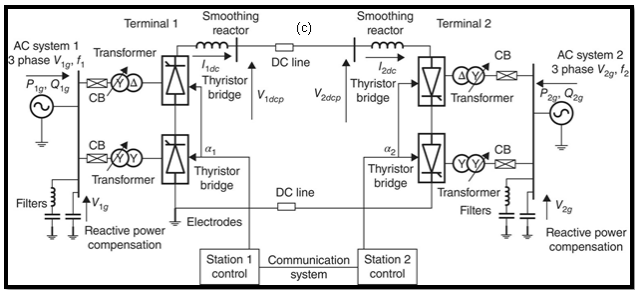

Figure 5 HVDC system

STUDY AREA AND METHODOGY

Four types of DC breakers and SFCL were modeled, and fault current interruption characteristics were compared to determine the HVDC CBs type most suitable for the application of SFCL considering the current interruption capability and reduction of total dissipated energy during DC fault.

Modeling of test-bed

HVDC Test-bed Model In order to analyze the impact of SFCL on various types of HVDC CBs, a test-bed model was designed in Matlab /Simulink as illustrated in Fig. The simple, symmetrical, monopole, point-to-point, 2-level, half-bridge HVDC system was utilized to concentrate the interruption performance of the DC fault current in detail. The AC network adjacent to the HVDC link was substituted by an equivalent RL impedance, which enabled the X/R ratio of the power system to be determined. The converter transformer was a wye-delta connection. A phase reactor was added between the converter and transformer to filter the harmonics during conversion. Each type of HVDC CB and SFCL was located at the output of the rectifier. Detailed specifications of the HVDC link are as follows: the rated voltage = ±100 kV, nominal current = 1 kA, nominal power flow = 100 MW, and the transmission line length = 50 km.

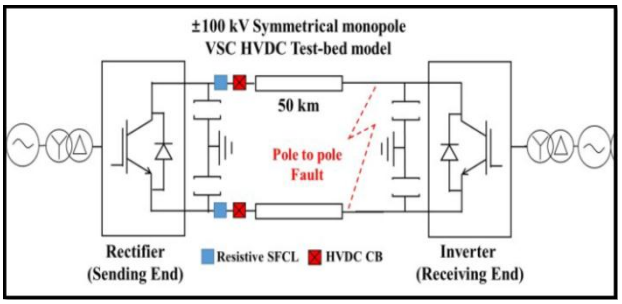

Figure 6 HVDC test bed model

Resistive Superconducting Fault Current Limiter

A **fault current limiter** (FCL), or **fault current controller** (FCC) is a device which limits the prospective fault current when a fault occurs (e.g. in a power transmission network) without complete disconnection.

The resistive SFCL, which is based on the quenching phenomena of superconductors, has been an area of great interest for researchers in the last decade and several prototypes have been developed and installed in medium- and high-voltage systems.

HVDC CBs

The simulation models of HVDC CBs in our simulation were designed as follows; Mechanical CB (MCB): This concept has been used for low-voltage DC breakers of few kilovolts only, which is usually in air-blast CB or SF6 CB. In case of MCB, a DC current is reduced by increasing the arc voltage to higher value than that of the system voltage. By utilizing the designed black-box arc model, the simulation model of MCB was designed as shown in Fig. (a). In order to achieve the practical approach of simulation results, the delay time was assumed as 10 ms.

Passive resonance CB (PRCB): To dissipate the energy stress on the MCB, the secondary path with a series L-C circuit is added as shown in Fig. (b). When the fault occurred at 0.1 sec, MCB opens with 10 ms of delay considering opening delay, and then an arc forms across the contacts with increasing arc impedance. The DC current begins to commutate and resonate in the secondary path after the arc impedance exceeds the L-C impedance. When a DC current of the primary path meets zero crossing, a current through the MCB can be interrupted by the extinction of the arc. An additional parallel surge arrester (SA) circuit is

supplemented to prevent voltage stress across the PRCB during arc extinction.

Inverse current injection CB (I-CB): This scheme is similar to PRCB. However, the pre-charged capacitor via an additional DC power source injects an inverse current into the primary path after the current commutates to secondary path as shown in Fig. (c). This can reduce the interruption and oscillation time when compared to that of PRCB. Before a fault, a charging switch (ACB1) and an auxiliary switch (ACB2) maintains closed state. Thereby capacitor can be charged by DC source. When a fault occurs, after an 10 ms delay, MCB and ACB1 contacts open simultaneously. Then the high discharging inverse current from capacitor is supplied to main path. The fault current is rapidly decreased and transient recovery voltage appears between the terminals of ICB. When the voltage exceeds to the knee voltage of SA, it is triggered to restrain the voltage rise, and it absorbs the fault energy. After 3 ms from the time when MCB and ACB1 were opened, ACB2 is triggered and it isolates the secondary path. This opening of ACB2 will prevent the current to flow through the secondary path which could make additional LC resonance current. Therefore, remaining fault energy is exclusively absorbed by SA. If the current reaches to zero, a residual circuit breaker (RCB) opens and the current interruption is complete.

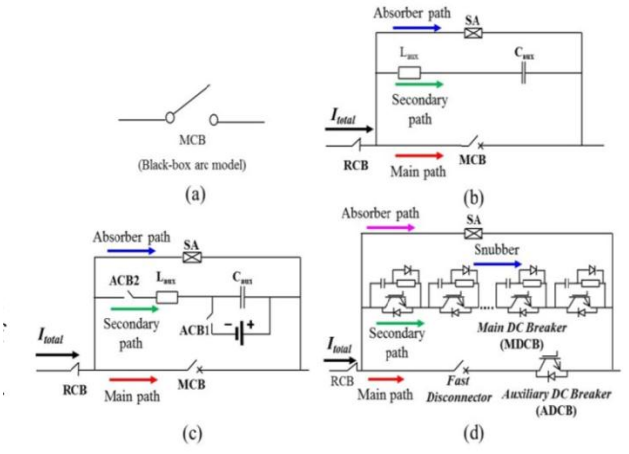

Figure-7 HVDCCBs

Hybrid DC CB (HDCCB): This scheme is widely considered as the optimal concept for interrupting DC fault current, was designed as illustrated in Fig. (d) . The delay times of IGBT was assumed as ΔtIGBT = 6 μs in simulation. When a DC fault occurs, the auxiliary DC breakers (ADCB) and fast disconnector are opened sequentially, then the current starts to commutate from the main path to secondary path. After commutation, main DC circuit breakers (MDCB) in secondary path are opened, and total current is reduced because the current flows to the snubber circuit of MDCB until the parallel-connected SA trips. When the voltage across the HDCCB terminals exceed to knee voltage, the SA ignites and forces the DC fault current to zero by absorbing remaining fault energy. Finally, a RCB opens and isolates the DC fault.

MODELLING AND SIMULATION

HVDC model with fault

Transient fault simulations were conducted to analyze the effects of SFCL on various HVDC CB types. Each type of HVDC CB, both with and without SFCLs, was applied at the sending end of the test-bed. A pole-to-pole fault, which considered a severe fault in HVDC systems, was generated on the receiving end at 0.1 sec.

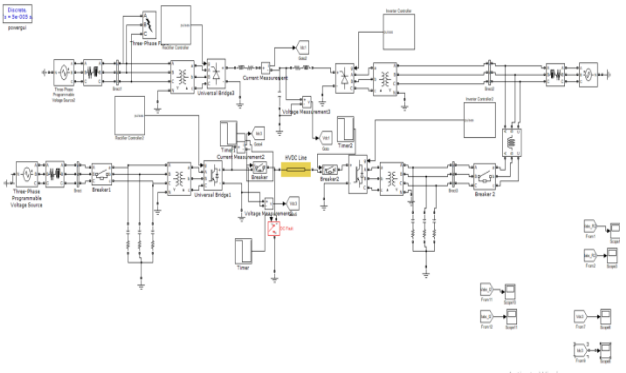

Fig-8 HVDC Main Proposed System

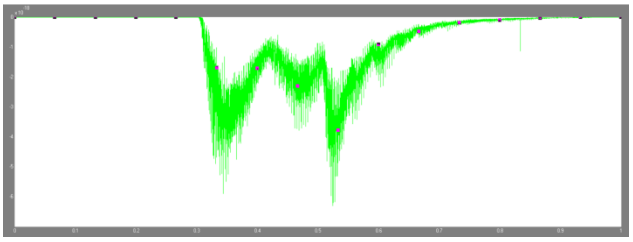

Fig-9 Inverse current flow after fault due to CB operation

In this work, we investigated application studies of resistive SFCL on the various types of HVDC CB in order to estimate the effects of combining fault current limiters and conventional DC breakers. Resistive SFCL have been acknowledged as an effective solution to effectively limit fault current levels by absorbing electrical and thermal energy stresses during fault. In this light, the combined application of SFCL and HVDC CB could be an attractive alternative solution capable of drastically decreasing the dissipated fault energy and improving the performance of HVDC CBs.

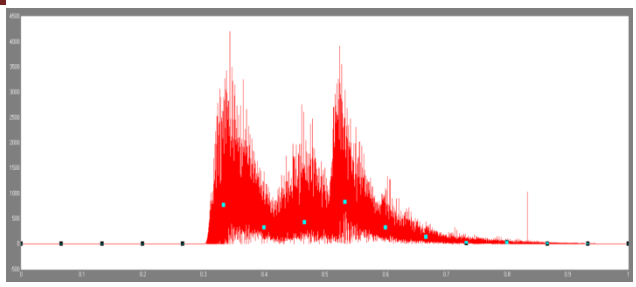

Fig-10 voltage rise after fault due to CB operation

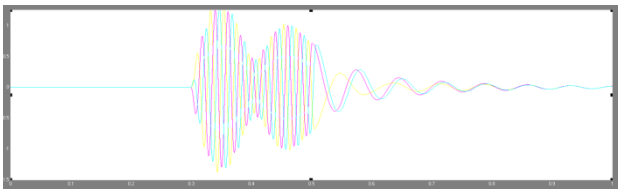

Fig-11 Voltage due to fault current

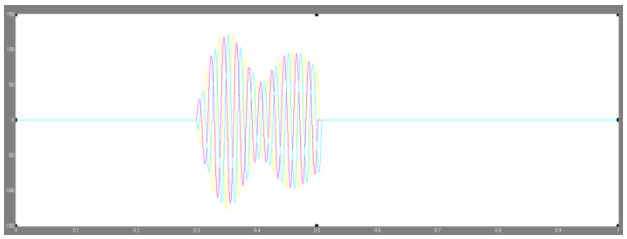

Fig 12 current due to fault current

Generally, fault current interruption can be easily achieved via zero-current crossing. While AC circuit breakers can interrupt a fault current in natural zero current, artificial current zero should be implemented for DC breakers to enable fault current interruption.

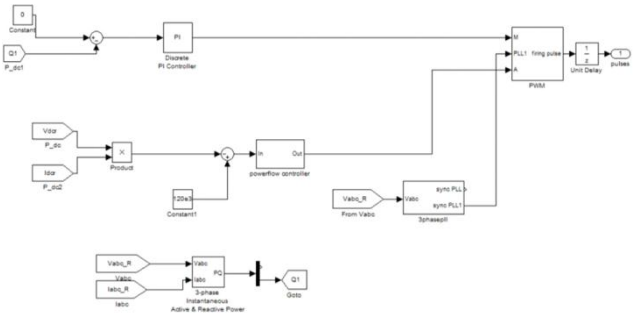

Figure 13 Sending end Control subsystem

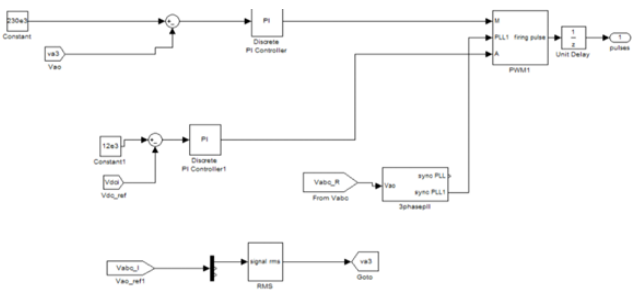

Figure-14 Receiving end control subsystem

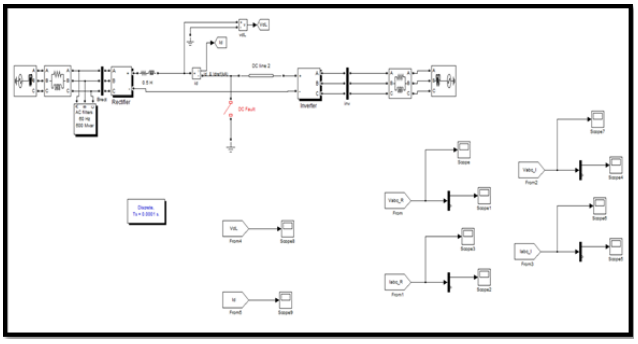

Fig-15 without STATCOM proposed System

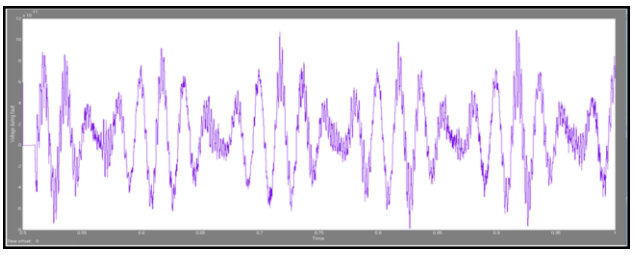

Fig-16 Voltage fluctuation

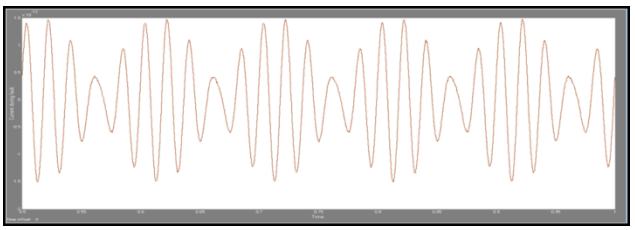

Fig-17 Current fluctuation

HVDC System with STATCOM

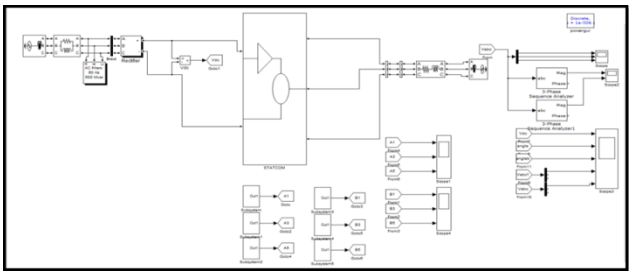

Fig-18 Proposed HVDC System with STATCOM

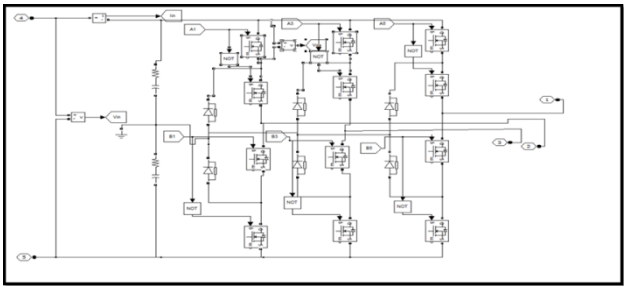

Fig-19 STATCOM Subsystem

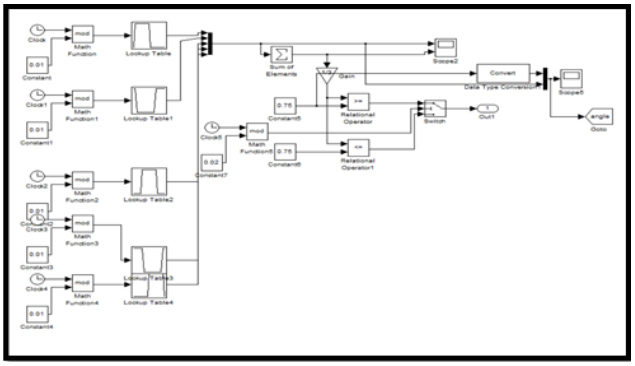

Fig-20 Control Subsystem for STATCOM Operation

In this section the STATCOM has been utilized for Analysis of fault in the proposed HVDC system. When we create the L-G fault in the HVDC line than the current and voltage fluctuation occurs which is shown in the fig above. Due to that stability of the proposed system has been disturbed. So, improve the stability and mitigate the fluctuation in voltage and current waveform. We have integrated the STATCOM device in the fault condition multi-grid HVDC system and simulation results in below section shows the improvements in the results.

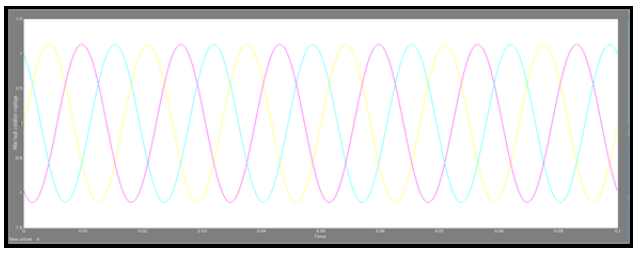

Fig-21 controlled Voltage after STATCOM Integration

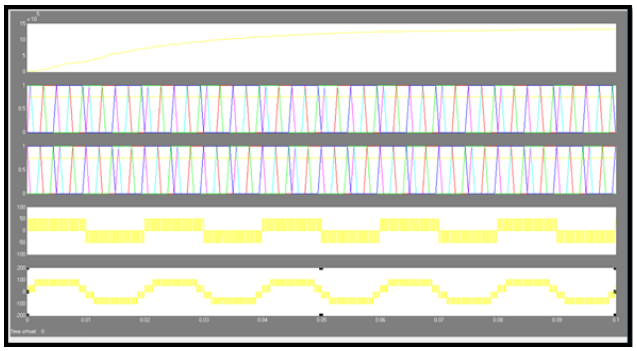

Fig-22 Final Controlled output of Proposed System

The STATCOM working as an effective device in the HVDC system as an inverter mode of operation compare to normal inverter. In the proposed system the STATCOM controlled the output parameters of the HVDC system and give the controlled output voltage at receiving end in the HVDC system. It has lower losses and good operating characteristic compare to other devices and normal inverter design in the system.

Multi Grid HVDC System with shunt STATCOM with Fault

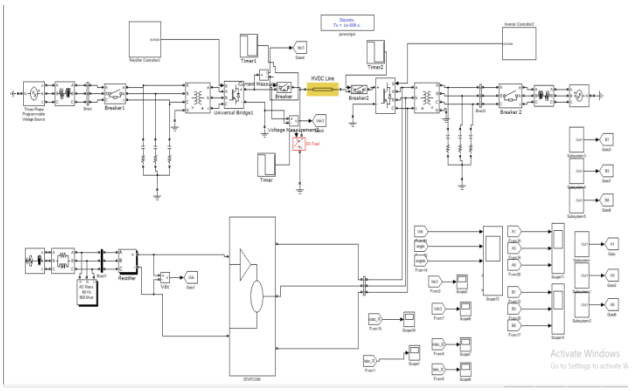

Fig-22 Proposed System with STATCOM Shunt Connection

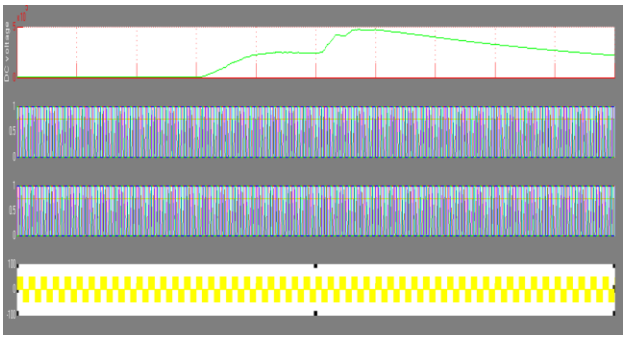

Fig 23-Final controlled Output of proposed system

CONCLUSION

This paper deals with the impact of SFCL on various types of HVDC CB. The resistive SFCL considers quenching characteristics and concepts of HVDC CB models including the black-box arc model, and a simple HVDC test-bed were designed using Matlab/Simulink. A severe DC pole-to-pole fault was imposed to analyze the interruption performance. From the simulation results, the maximum fault current, interruption time, and dissipated energy stress on an HVDC CB could be decreased by applying an SFCL. Noticeable enhancement of the fault interruption capability was exhibited by PRCB, which showed the longest interruption time and highest maximum fault current without SFCL. When the SFCL was applied, the L/R time constant of the secondary path was decreased, and therefore fast interruption with less oscillation was observed. Consequently, SFCL installation with PRCB could be a viable, reliable, and cost-effective option to enhance DC fault current interruption capability

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