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A Comparative Study of Multilevel and Conventional Inverters

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Abstract – From the past couple of decades, multilevel inverter technologies are suitable for high power industrial applications. Multilevel inverter synthesizes several DC sources. Multilevel inverter is the most suitable technology for conversion in renewable sources. This study which discussed about Multilevel Inverter Topologies, Topology Comparison, Simulation and Analysis, Multilevel inverter topology and a comparative study of Multilevel inverter topologies in terms of number of switches, harmonic content and efficiency. These topologies are cost effective as compare to conventional multilevel inverters. Despite of many advantages, multilevel inverter with reduced switches basis some advantages like the voltage stress on the individual switches increases. For that, it is recommended to use switches of high rated values. All the topologies are modelled using Matlab/Simulink and the results are validated and compared.

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I. INTRODUCTION

Multilevel inverters include an array of power semiconductors and capacitor voltage sources, the output of which generate voltages with stepped waveforms. The term multilevel starts with the three-level inverter introduced by Nabae et. al. [1]. By increasing the number of levels in the inverter, the output voltages have more steps that is, a staircase waveform, with reduced harmonic distortions. A multilevel inverter has several advantages over a conventional two-level inverter that uses high switching frequency pulse width modulation (PWM). The main attractive features of a multilevel inverter are[1]:

1) **Low dv/dt stress**: Multilevel inverters not only can generate the output voltages with very low distortion but also can reduce the dv/dt stresses.

2) **Common-mode (CM) voltage**: Multilevel inverters produce smaller CM voltage; therefore, the stress in the bearings of a motor connected to a multilevel motor drive can be reduced.

3) **Input current**: Multilevel inverters can draw input current with low distortion.

4) **Switching frequency**: Multilevel inverters can operate at both fundamental frequency and high switching frequency PWM. It should be noted that lower switching frequency usually means lower switching loss and higher efficiency.

Multilevel inverters do have some disadvantages. One being the requirement of many power semiconductor switches. Also each switch requires a related gate drive circuit. This may cause an increase in overall expenses of the system.

II. MULTILEVEL INVERTER TOPOLOGIES

Multilevel inverters can be mainly divided into three major types:

1) *Cascaded H-bridge multilevel inverters*: These inverters include several H-bridge cells (Full-bridge inverters) connected in series.

2) *Diode-clamped multilevel inverters*: These inverters use clamped diodes and dc capacitors in order to generate ac voltage. This structure is known as neutral-point clamped (NPC) and is widely used in medium voltage, high power drives.

3) *Flying-capacitor multilevel inverter*: In this topology, semiconductor devices are in series and their connecting points are clamped by extra capacitors.

2.1. Cascaded H-bridge Multilevel Inverter

A structure of an m-level cascaded inverter is shown in Fig.1. Each separate dc source (SDCS) is connected to a H bridge inverter. The number of output phase voltage levels, *m*, is given by *m = 2s+ 1*, whereas is the number of separate dc sources[2]. Cascaded inverters have been used for such applications as static var generation, with renewable energy sources, and in battery-based applications. The main advantages and disadvantages can be listed as[4]:

Advantages:

- The number of possible output voltage levels is more than twice the DC sources (m = 2 s + 1).
- The series of H-bridges shows a modularized layout and packaging. This will enable the manufacturing process to be more quickly and cheaply.
- Possibility of soft-switching.
- Simple voltage balancing.

Disadvantages:

- Separate DC sources are required for each of the H bridges. This will limit its application to products that already have multiple SDCSs readily available.
- No common DC-bus.

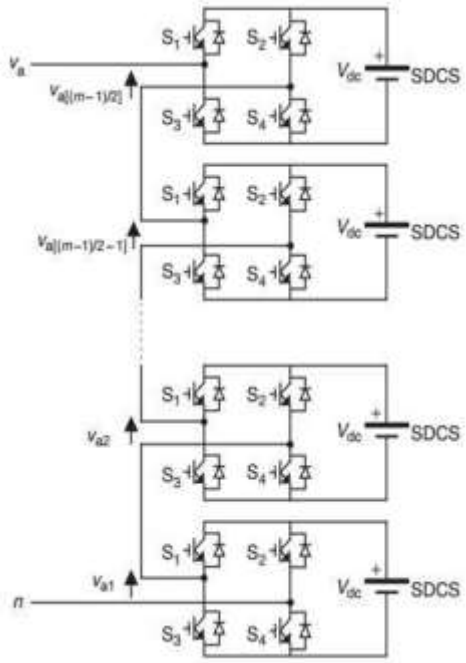

Fig. 1. Structure of a multilevel cascaded H-bridge inverter [2]

2.2. Neutral point clamped Multilevel Inverter

A common DC-bus is divided by bulk capacitors in series with a neutral point in the middle of the line.

The number of capacitors depends on the number of voltage levels in the inverter. From this DC-bus, with neutral point and capacitors, there are clamping diodes connected to an (*m* − 1) number of switch pairs, where m is the number of voltage levels in the inverter.

One application of the multilevel diode-clamped inverter is an interface between a HV dc line and an ac line. Another would be a variable speed drive for high-power medium voltage motors. The main advantages and disadvantages of this inverter as follows:

Advantages[8]:

- All the phases share a common dc bus, which minimizes the capacitance requirements of the converter.
- The capacitors can be precharged as a group.
- Efficiency is high for fundamental frequency switching

Disadvantages:

- Real-power flow is difficult for a single inverter.
- The number of clamping diodes required is quadratically related to the number of levels.

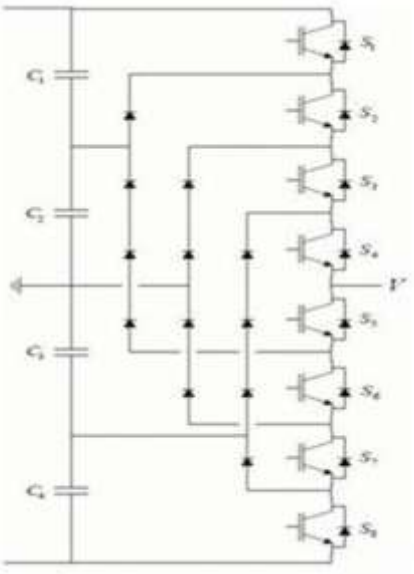

Fig. 2. Seven level diode clamped inverter[5]

2.3. Flying-capacitor Multilevel inverter

The structure of this inverter is similar to that of the diode-clamped inverter.Only difference is that instead of using clamping diodes, the inverter uses capacitors. The voltage on each capacitor differs from that of the next capacitor. The voltage increment between two adjacent capacitor legs gives the size of the voltage steps in the output waveform. The voltage synthesis in a seven-level capacitor-clamped converter has more flexibility than a diode clamped converter.

Similar to neutral point clamped inverter, the capacitor clamped inverter requires a large number of bulk capacitors of voltage clamping. The voltage rating of each capacitor used will be the same as that of the main power switch, therefore, an m-level converter will require a total of (m − 1)(m − 2) /2 clamping capacitors per phase leg in addition to (m − 1) main DC-bus capacitors. The advantages and disadvantages of capacitor clamped inverters are given below[4].

Advantages:

- Phase redundancies are available for balancing the voltage levels of the capacitors.
- Real and reactive power flow can be controlled.
- The large number of capacitors means the inverter can ride through short duration outages and deep voltage sags.

Disadvantages:

- Control is complicated to observe the voltage levels for all of the capacitors. Pre charging all of the capacitors to the same voltage level and startup are complex.
- Switching utilization and efficiency are poor for real power transmission.
- The more number of capacitors are both more expensive and bulky than clamping diodes in multilevel diode clamped converters. Packaging is also more difficult in inverters with a high number of levels.
- Complicated control, leading to high switching frequency and losses, when transferring real power.

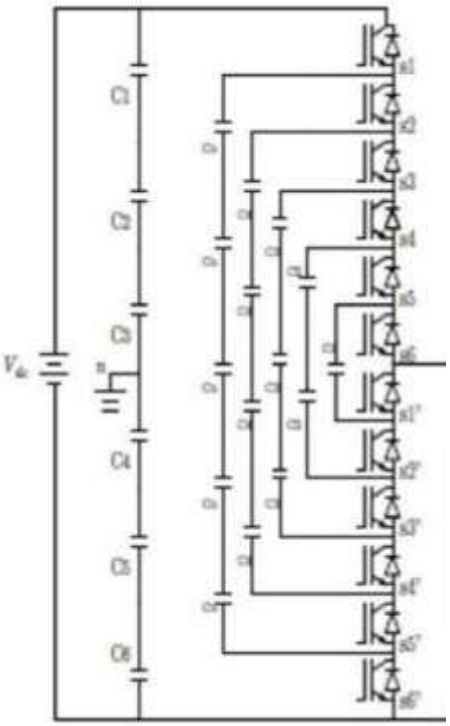

Fig. 3. Seven level capacitor clamped inverter

2.4. A New Topology with Reduced number of Switches

Figure 4 shows the proposed novel topology used in the seven level inverter. An input voltage divider is composed of three series capacitors C1, C2, and C3. The divided voltage is given to H-bridge by four MOSFETs, and four diodes. The voltage is send to output terminal by H-bridge which is formed by four MOSFETs. The proposed multilevel inverter generates seven-level ac output voltage with the appropriate gate signals design. The purpose of the multilevel topology is to reduce the voltage rating of the power switch. By combining output voltages in multilevel form,shows advantages of low dv/dt, low input current distortion, and lower switching frequency. The major feature of the proposed topology is the reduction of power components.

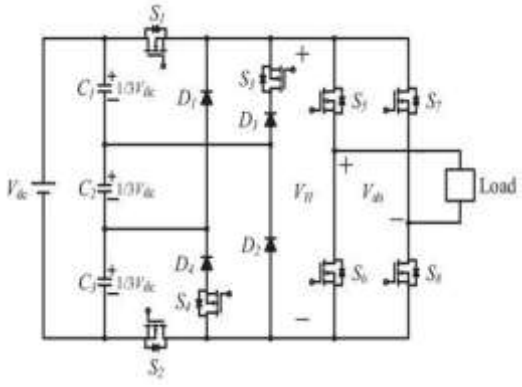

Fig. 4. Seven level Inverter with reduced number of switches[3]

III. TOPOLOGY COMPARISON

Comparison of multilevel inverter is made based on the following criteria's:

- Number of semiconductor devices used per phase leg.
- Number of DC bus capacitors used.
- Number of voltage balancing capacitors used per phase.
- Amplitude of fundamental and effective harmonic components.
- Total Harmonic Distortion of output voltage.
- Control complexity based on voltage unbalances of power switches.
- Cost estimation in designing of power circuit and the associated components.

Table 3.1 Comparison of different multilevel inverter topologies

Topology	Diode clamped	Capacitor clamped	Cascaded
Power Semiconductor switches	2(m-1)	2(m-1)	2(m-1)
Clamping diodes per Phase	(m-1)(m-2)	0	0
DC bus capacitor	(m-1)	(m-1)	(m-1)/2
Balancing capacitor per phase	0	(m-1)(m-2)/2	0
Voltage Unbalancing	Average	High	Very small

By comparing the number of devices needed, it can be seen that the proposed topology has much less number than the others.

Table 3.2. Comparison of number of devices

Devices	New Topology	Diode clamped	Capacitor clamped	Cascaded
Input Sources	1	1	1	3
Input capacitors	3	6	2	3
Clamped capacitor	0	0	5	0
Power switches	8	12	12	12
Diodes	4	10	0	0

IV. SIMULATION AND ANALYSIS

Matlab Simulation of 3-Level Inverter

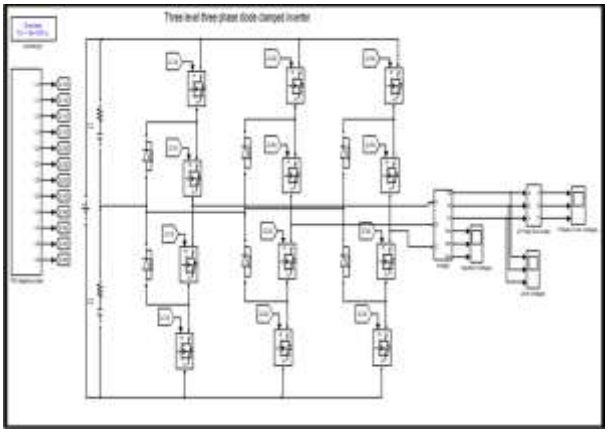

Fig 5- Matlab Simulation Model of 3-Level Inverter

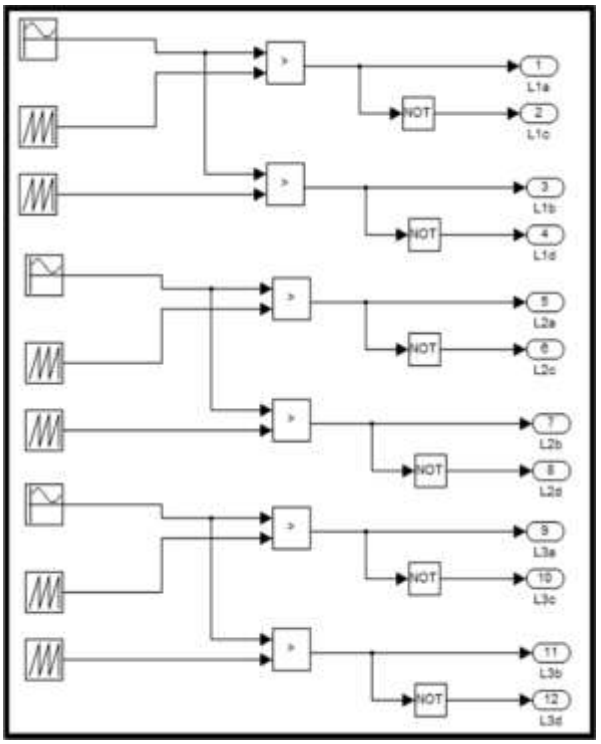

Fig 6- Controlling Subsystem

The three phase three level cascaded multilevel inverter is constructed by combining the H bridges of (n-1) numbers.

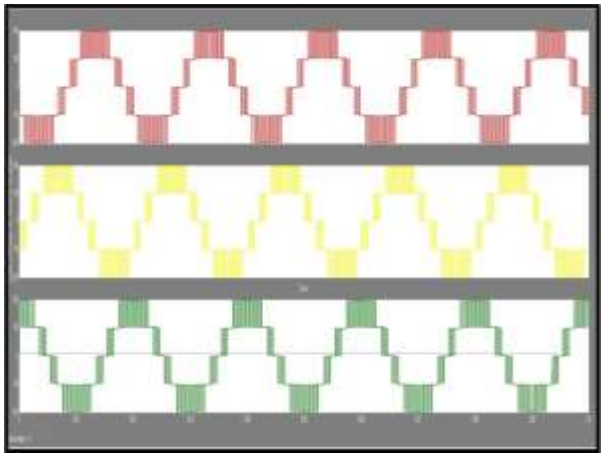

Fig 7- Three level Inverter Output Line Voltages

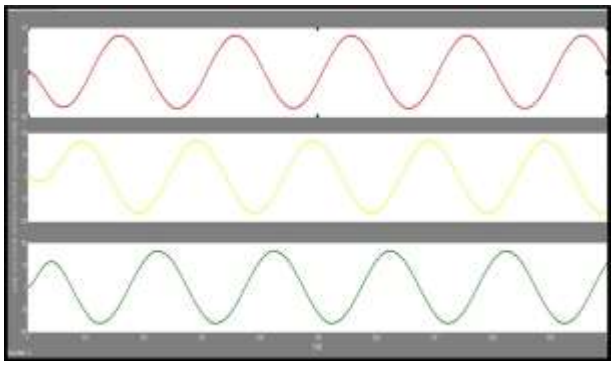

Fig 8- Filter Output Voltage of Inverter

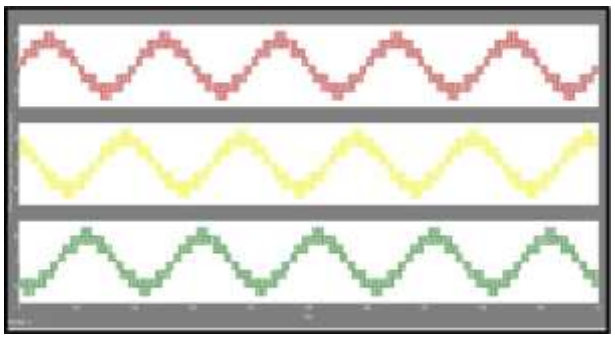

Fig 9- Phase Voltage of 3-level Inverter Output

Matlab Simulation of 7-Level Inverter

In seven-Level Asymmetrical Inverter each leg of a single phase contains 2 DCVS (DC Voltage Source) of 100V and 200V unlike the 3 DCVS of 100V each in 7-Level Symmetrical Inverter. This arrangement thus reduces the number of voltage supplies used.

To prevent commutation errors, same switching pulses are provided to IGBT (1, 2), (3, 4), (5, 6), (7, 8) and so on in the other two phases as well. Due to the different input voltages of the cells, high-voltage switches presenting low relative conduction losses are combined with low-voltage switches having low commutation time. Naturally, for most operating points, the switching frequency of low voltage cells is higher. Together with the switch characteristics, one can take advantage of this specificity.

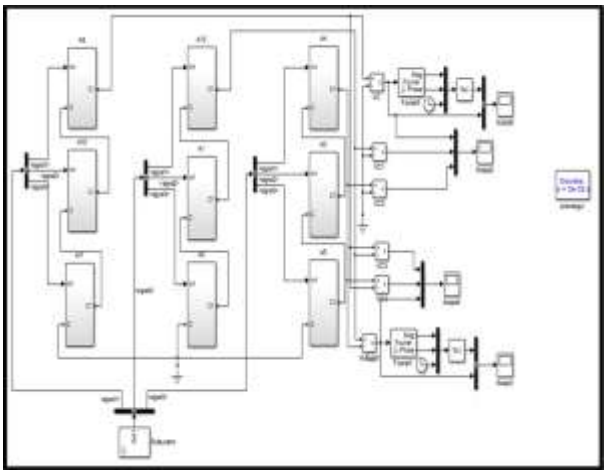

Fig 10 Matlab Simulation Model of Seven Level Inverter

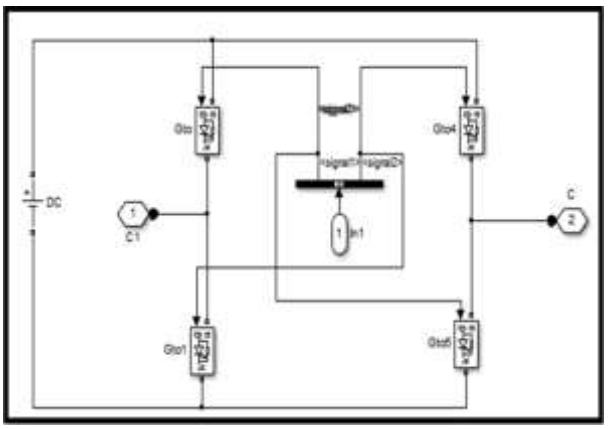

Fig 11Subsystem of Each Switching block

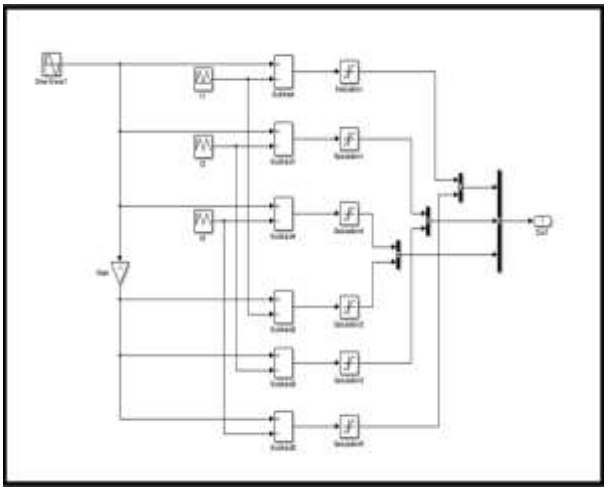

Fig 12-Controlling subsystem of 7-Level Inverter

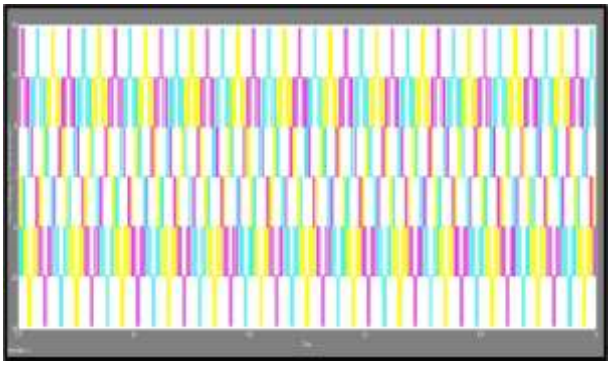

Fig 13- : Line-Line Voltage Waveform of 7-level inverter output

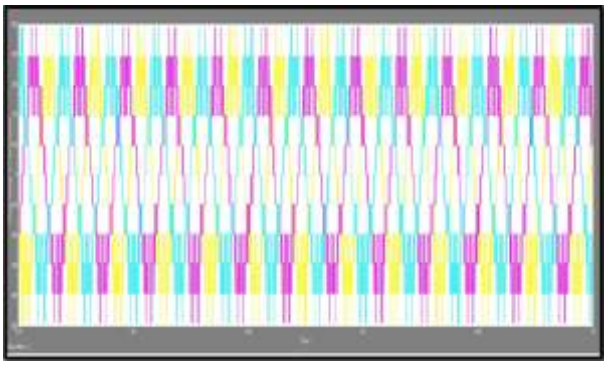

Fig 14- Phase Voltage Waveform of 7-level inverter output

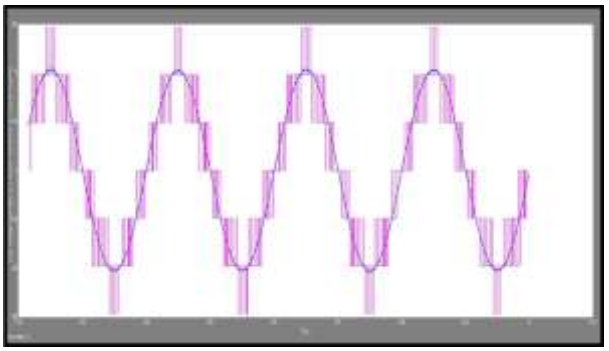

Fig 15 Line voltage and filter A.C output waveform of 7-Level Inverter

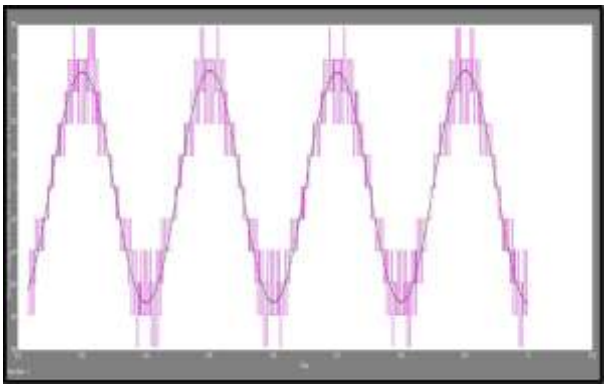

Fig 16 Phase voltage and filter A.C output waveform of 7-Level Inverter

Fig 17 Line-Line Voltage Waveform of 7-level inverter output with zoom scale

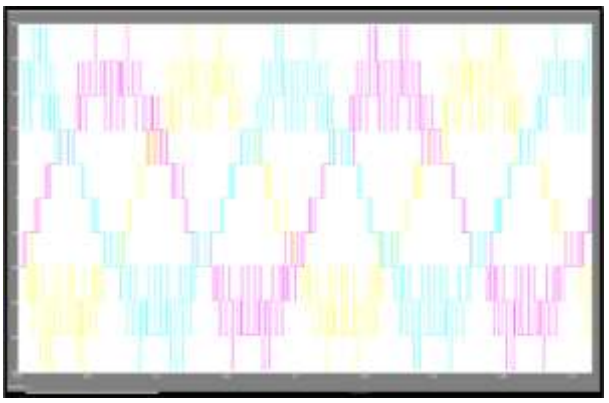

Fig 18- Phase Voltage Waveform of 7-level inverter output with zoom scale

V. CONCLUSION

Various Multilevel inverter topologies were studied using simulation results. The three level, seven level cascaded H-bridge inverters were simulated in MATLAB-Simulink environment. Two types of Multicarrier Pulse Width Modulation – Level Shifted Modulation and Phase Shifted Modulation were implemented for the cascaded multilevel inverter. It was found that the cascaded rectifier inverter configuration gave sinusoidal output waveform. This converter system can meet the power or voltage requirement of the traction drive. The cascaded eleven level converter system modeled in this project can be used in traction drive consisting of four induction motors for stepping down the catenary voltage to the rated voltage of the induction motors.

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