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Study of Dual Gate Mosfet over Digital Application

Ritu Kaundilya[1]*, Dr. Arun Kumar[2]

[1] Research Scholar, A.N. College Boring road Patna India

[2] Research Guide, Electronics Department, A.N. College Boring road Patna India

Email id: ritukaundilya@gmail.com

Abstract - This paper is dedicated to a thorough investigation of the dual-gate metal-oxide-semiconductor field-effect transistor (MOSFET) and its potential digital-age applications. The dual gate metal- oxide-semiconductor field-effect transistor (MOSFET) is a voltage-controlled dual material gate (DMG) structure that may boost the efficiency, performance, and functionality of electronic circuits in the nanotechnology, microprocessor, wireless communication, etc. industries.

Dual gate MOSFET has the ability to enhance digital application capabilities in the present revolutionary era. The exact circuit performance of a dual gate MOSFET may be examined digitally, revealing its unique properties. This may have far-reaching consequences for the digital world in terms of power use, power efficiency, memory chip density, switching speed, etc. Using features technology, we may circumvent transistor loss due to load settings and other things. By switching to a dual-gate MOSFET, we were able to fix the issue and boost the circuit performance beyond that of a single-gate CMOS design.

PSPICE simulation software was used to get these findings, and the Equivalent circuit approach was used to analyze the properties and performance of the dual gate MOSFET. Take into account the fact that attributes might vary depending on context. Trans capacitance as a function of gate voltage, threshold voltage as a function of lateral straggle parameter and temperature, mobile charge density as a function of temperature, etc., are some examples of the behaviors of parameters that are examined. When compared to earlier theoretical research, the outcome gained with digital application is easier to grasp.

Keywords - dual gate MOSFET, PSPICE Software, Trans capacitance, Threshold voltage

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1. INTRODUCTION

Since the early 1970s, the steady miniaturization of the MOSFET, the semiconductor's fundamental building block, has been directly linked to the industry's progress toward large- scale integration of metal oxide semiconductors. If the area of the chip must remain constant, then decreasing the size of the MOSFETs is the best and most effective approach to improve performance, increase packing density, increase the number of functions in a given chip area, and reduce power consumption. Due to short channel effects, smaller MOSFETs have different electrical properties than their larger size equivalent. In order to meet the needs of the modern electronics industry and render MOSFETs amenable to ultra-large-scale integration, it is necessary to introduce cutting-edge technologies, unconventional architectures, and unique materials. Literature has suggested a multi-gate field-effect transistor (MUGFET) in which the gates exert additional electrostatic control over the channel. The literature suggests a junction- less transistor as a possible solution to the heat budget issue in steep S/D junction creation. Reduced ON-state current and transconductance are the consequence of mobility deterioration in the severely doped channel of the JL MOSFET. Since the JL MOSFET operates on bulk conduction, the channel must be entirely depleted while the device is in its off state, which necessitates gate metal with a larger work function.

As such, the addition of two binary digits is a crucial task for every computer processor. Despite the growing popularity of clockless/asynchronous processors/circuits, the vast majority of adders have been developed utilizing synchronous circuits. When it comes to timing, asynchronous circuits are the most common kind. Since they lack the drawbacks of timed (synchronous) circuits, they provide a huge opportunity in logic design. For the most part, request acknowledgment handshaking Protocol signals are used to form a pipeline in asynchronous circuits, allowing them to function without clocks.

Explicit handshaking blocks, like bit adders, are very

inexpensive but yet include a set of tiny, individual components. So, utilizing dual-rail carry propagation in adders, it is handled implicitly and effectively. A single-bit adder block's valid dual-rail carry output serves as both an acknowledgement and data signal. Therefore, asynchronous adders are founded on either full dual-rail encoding of all signals (in a more formal sense, using null convention logic, which employs symbolically correct logic in place of Boolean logic) or pipelined operation based on single-rail data encoding and dual-rail carry representation for acknowledgment signals. These structures improve circuit designs' resilience but also add a lot of unnecessary complexity, which hurts asynchronous adders' performance on average.

2. LITERATURE REVIEW

Mukherjee, M., Guha, S., Debnath, P. *et al.* (2022) In this study, we provide a unique configuration of doping-less double-gate Impact ionization metal-oxide-semiconductor field- effect transistors (DL DG IMOS) based on the impact ionization principle, implemented on p- type Si material. Impact ionization and the use of a silicon layer provide for a simpler construction procedure, while also enhancing the device's subthreshold properties. Unique to this device is the absence of metallurgical connections and impurity doping in the source and drain regions. Extensive simulations in SILVACO TCAD have verified the accuracy of the mathematical models offered here. Reduced thermal budgeting and steeper SS slopes are two of the many ways in which the results and simulation show this device to be useful for high switching applications.

Jaiswal, Sushmita & Gupta, Santosh. (2022) Typical Double Gate (DG) MOSFETs have challenges, such as heightened Short Channel Effects (SCEs). In this work, a Core Insulator Double Gate (CIDG) MOSFET with an engineered channel is presented for use in low-power digital circuits. An insulating material is used to line the channel's interior in the suggested device. A considerable decrease in leakage current is achieved with the use of a rectangular core insulator, which has a positive effect on the device's performance metrics. After confirming the consistency between the simulation findings and the DG MOSFET reference data, the structure is analyzed. It has been shown that at 20 nm, CIDG MOSFETs have lower I off, higher Ion/I off, better Drain Induced Barrier Lowering (DIBL), and steeper Sub-threshold Slope (SS). For a CIDG MOSFET with a 20 nm channel length, the returned values for I off, Ion/I off, SS, and DIBL reveal decreases of 59.101%, increases of 136.077%, decreases of 4.018%, and increases of 34.753%, respectively. Furthermore, the CIDG MOSFET has enhanced transconductance generation factor, output conductance, intrinsic gain, early voltage, and cut off frequency.

Qingguo Gao (2021) 2D molybdenum disulfide (MoS2) has shown promising results as an atomically thin semiconductor for developing next-generation logic circuits, RF devices, and flexible electronics. There are a number of techniques that have been used to enhance the high- frequency properties of MoS2 RF transistors, but little is known about how the back-gate bias affects dual-gate MoS2 RF transistors. We investigate the impact of back-gate control on static and RF performance parameters in MoS2 high-frequency transistors. Top-gate transistors with an on/off ratio of 107 and an on-current of up to 179 A/m at room temperature were accomplished by using high-quality chemical vapor deposited bilayer MoS2 as the channel material. At Vbg = 3 V, the on-current climbs to 278 A/m while the source- and drain-contact resistances drop to 1.99 km thanks to the back-gate modulation. When the back-gate voltage is raised to 3 V, the cut-off frequency and the maximum oscillation frequency both rise. Additionally, an intrinsic fmax maximum of 29.7 GHz was attained, which is as much as 2.1 times the fmax without the back-gate bias. This study demonstrates the promise of dual-gate MoS2 RF transistors for future high-frequency applications and sheds light on the impact of back-gate voltage on MoS2 RF transistors.

Sarita Misra (2021) Using the ATLAS TCAD device simulator, this article investigates the potential benefit of surrounding gate junction less graded channel (SJLGC) MOSFET from the standpoint of its Analog, RF performances. Systematically, the effects of a laterally graded channel on the potential, electric field, and velocity of carriers, and the energy band along the channel are studied. The present study focuses primarily on the improved performance of SJLGC MOSFET as shown by its increased drain current (ID), transconductance (gm), cut-off frequency (ft), maximum oscillation frequency (fmax), and critical frequency (fK). Grading the channel has an effect on SJLGC MOSFET, increasing the drain current by 10.03 percent. The ft, fmax, and Fl characteristics of SJLGC MOSFETs have increased by 45%, 29%, and 18%, respectively, indicating superior RF performance. The SJLGC MOSFET outperforms the SJL MOSFET in the sub-threshold region, as shown by a 74% increase in intrinsic voltage gain (gm/ gds). On the other hand, at the subthreshold region, the transconductance generation factor of SJLGC MOSFET is less than that of SJL MOSFET. When compared to SJL MOSFET, SJLGC MOSFET has a reduced intrinsic gate delay (D) because to the influence of lower gate to gate capacitance (CGG), which suggests superior digital switching applications. Based on the simulation findings, SJLGC MOSFET has the potential to be used in a variety of next- generation RF circuits over a wide frequency range.

R.Vigneshwari (2017) Here we provide a recursive formulation for multi-bit binary addition that is implemented in a parallel single-rail self-timed adder using dual gate MOSFETs. With no requirement for specialized speedup hardware or look-ahead design, the circuit achieves logarithmic performance

over random operand circumstances by performing addition in parallel for those bits that do not need carry chain propagation. There is a completion detecting unit and a useful design for a dual gate MOSFET. Consistent with no real restrictions on high fan outs, the design is straightforward. Due to the nature of asynchronous logic, the design must have a high fan-in gate, which is handled by placing the transistors in parallel. The feasibility and superiority of the proposed technique over preexisting asynchronous adders have been validated using simulations run with the LT spice tool.

3. TUNABLE CURRENT MIRRORS

One of the simplest and most crucial building parts of an analog circuit is the current mirror (CM; see Fig. 1. Reference currents can be replicated across I/A blocks, and operating points may be programmed. Once the circuit is constructed, the ratio of transistor width between the input (reference) and output branch is fixed, allowing the mirror properties to be defined. However, as shown in Fig. 1, by using the correct bottom biases of the DG-MOSFETs utilized in the mirror block, a comparable gain factor may be readily produced, and dynamically modified (b). This basic circuit's tunability not only expands its potential uses but also has the potential to result in space and/or power savings in comparison to equivalent circuits designed using bulk MOSFETs. It is feasible to get mirror ratios close to 100 even at relatively low bottom-bias conditions at the output transistor (Vseto B 1 V). Figure 1 illustrates this by showing the relationship between the output current (Iout) and the output node (Vout) for a variety of input voltages (Iin) (Vseto). Figure 2 depicts the relationship between output current and setting voltage (Vseto) for a range of input currents (Iin). This picture includes an inset illustrating the relationship between the bottom-gate setting voltage and the current ratio.

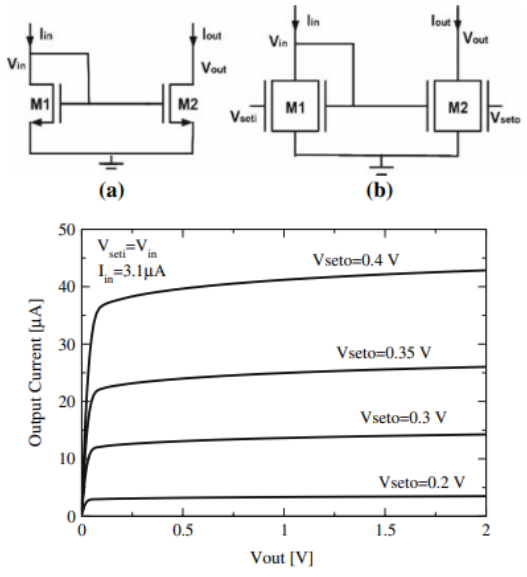

Fig. 1 Simple current mirror based on conventional CMOS transistors. (b) Simple current mirror based on DG-MOSFET. (c) The output current versus output voltage for DG-MOSFET simple current mirror

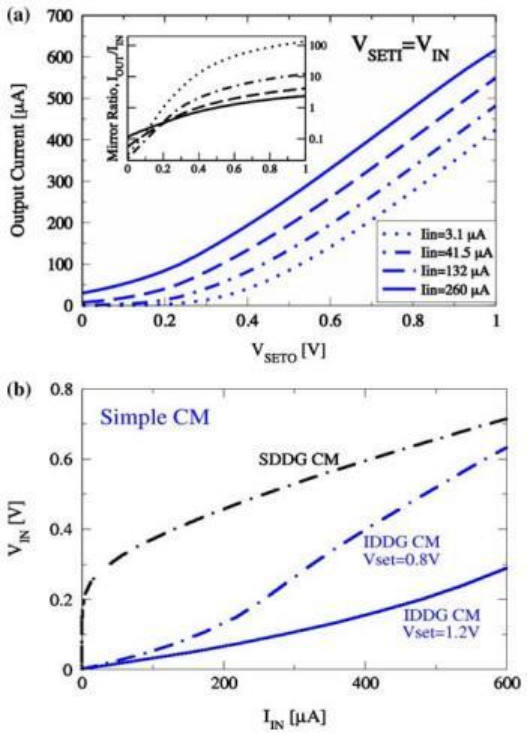

Fig. 2 Output current for different reference voltage Vref (e.g., IIN) versus output setting-voltage (Vseto).

The mirror's output-to-input ratio is shown in the inset. A comparison of the voltage needed across the input transistor in the basic DG current mirror while using two different bias voltages for the IDDG and the regular SDDG. Less power is required from the input when the bottom gate bias is increased.

Comparatively, the voltage across the input DG device mirror in a tunable DG CM circuit is much less than the voltage needed for a traditional MOS current mirror in a simulated SDDG arrangement (Fig. 2). If you compare the output impedance of the basic CM to the samples shown in Fig. 1 by Kumar et al, you'll see that the latter are noticeably lower while the latter are higher. Since the prior study relied on 1 lm DG-MOSFETs rather than the 100 nm devices employed here, the models used there were not able to adequately account for short channel effects. Reducing output resistance explains how our TCAD analysis overcomes short channel effects. The modified cascade CM in Fig. 3 is well-suited for low-voltage operation and may be used to compensate for the loss of output conductance. As can be seen in Fig. 3, the cascade CM design improves output while keeping all of the tuning features of the basic CM (b). Also, the supply voltage is unaffected by this save for a little increase compared to basic CM. Once again, Fig. 4 compares the cascade IDDG CM to the traditional (SDDG) scenario, demonstrating the low-voltage (and low-power) potential of the IDDG arrangement by contrasting the needed voltage across the two input

devices (M1 and M2 in series).

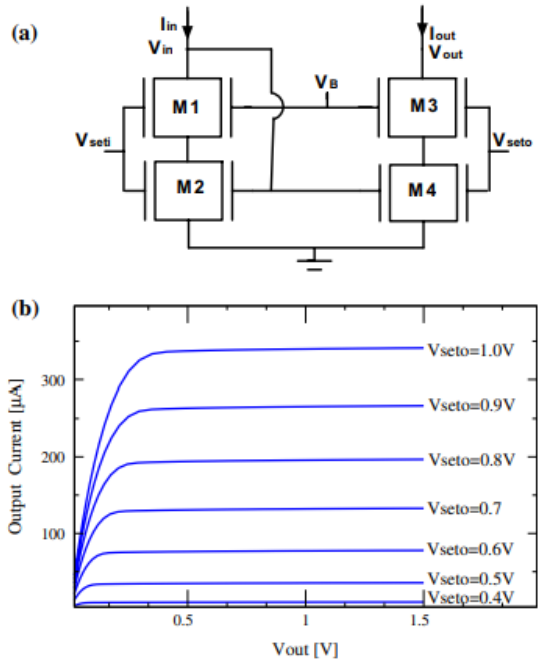

Fig. 3 Cascade current mirror based on DG-MOSFET (b) Output current versus output voltage for DG-MOSFET cascade current mirror at IIN = 130 LA and Vseti = 0.8 V

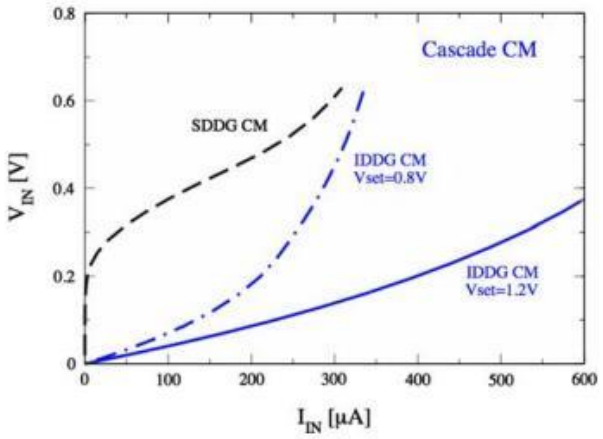

Fig. 4 Comparison of the required voltage across the input transistors of the cascade DG current mirror in three configurations

The simulation findings demonstrate that the DG current mirror outperforms the standard MOS current mirror in many key respects, including reduced power consumption, reduced voltage requirements, and the elimination of a second transistor for tuning (less area and parasitic). The next sections study more complex current-mode circuits blocks, which employ a number of such CM in differential topology to create amplifiers and filters, and where the knowledge gained from the CM circuits will be useful.

4. CONCEPT OF DEVICE MODEL AND THE EQUIVALENT CIRCUIT MODELING

4.1 Device modeling of Vertical IMOS

Using ORCAD PSPICE simulation, a vertical IMOS model is created (based on level 3). Given its sensitivity to the threshold voltage, level 3 was chosen as the MOSFET model's parameter. The electrical properties and characteristics of each component serve as the model for the electronic circuit. Vertical IMOS, suggested by U. Abelein, will be compared to experimental values using the device's characteristic graph (IDS-VGS).

Here are the equations used to establish the parameters of the MOSFET model at the third- level. To determine the VTH threshold voltage

$$V_{TH} = V_{TO} - \gamma\sqrt{2\varphi_f} + \gamma F_t\sqrt{2\varphi_f + V_{SB}} + F_w(2\varphi_f + V_{SB}) - \sigma V_{DS}$$

$$\text{where}\sigma = \frac{8.15^{-22}\eta}{C_{ox}L^3}$$

The bulk Fermi potential is denoted by, while the body factor is shown by. The factor is a narrow width factor, whereas the factor is a short channel factor. Current ON may be calculated by fitting the graph into the linear area where the drain current equation holds;

$$I_D = \beta(V_{GS} - V_{TH} - \frac{1+F_B}{2}V_{DS})V_{DS}$$

$$\text{where } \beta = \frac{W}{L}\mu_{eff}C_{ox}$$

$$F_B = Taylor\ series\ expansion\ coeeficient\ of\ bulk\ charge$$

The subthreshold zone of the graph depicts the off state of the current,

$$I_D = I_o \exp\left[\frac{q}{kT}\frac{V_{GS}-V_{ON}}{n}\right]$$

Where

$$V_{ON} = V_{TH} + \frac{nkT}{q}$$

$$n = 1 + \frac{qNFS}{C_{ox}} + \frac{C_D}{C_{ox}}$$

In the meanwhile, ORCAD PSPICE uses the factory default setting for the BJT parameter. The gate, source, and drain losses are modeled by adding three more resistors to the circuit. The impact of drain and source resistance on overall device performance must be carefully monitored when MOSFET scaling approaches the micrometer range.

Specifically, it is known that the Rs and Rd rely on gate bias in MOSFETs. Unlike Rd, Rs is more of a determining factor in the electrical performance and dependability of the device, as well as its saturated drain current (Ion), trans-conductance (gm), noise figure, cutoff frequency, and hot carrier degradation effects.

Finally, the capacitor circuit is given the gate-source voltage and drain-source voltage. On the other hand, the intrinsic resistances employed to improve the fitting quality at high frequencies. Capacitor Ci1 represents the oxide-based intrinsic layer between the drain and the body, while Capacitor Ci2 represents the second layer between the body and the source.

Figure 3 depicts the equivalent circuit model of a vertical IMOS, which comprises of n- MOSFET and NPN BJT, as well as certain parasitic components in the form of capacitances and resistors. Because it was derived from an experimental value, the parameter of the modeled device cannot be changed. The ideal width (W) is set to about 1000nm, the substrate doping (NSUB) is 109 cm-3, the oxide thickness (TOX) is 4.5nm, the channel length (L) is 83nm, and the threshold voltage (VTO) is 1.3V, all based on the cited experimental result.

Unlike its planar counterparts, vertical IMOS perform a variety of tasks. In a vertical IMOS, there are three distinct operational modes that may exist at any one time. In order: CMOS (common metal oxide semiconductor field effect transistor), II (impact ionization), and BJT (bipolar junction transistor). The voltage delivered to the device's drain determines the mode it operates in.

The transfer characteristic curve is shown in Figure 4 and was derived using the comparable circuit and device modeling approach. As long as VDS is below 1.5V, the component operates in CMOS mode. Energy levels are too low to trigger the II at the current pace. For a subthreshold slope of 76.58mV/dec at VDS=1.25, and 72.89mV/dec at VDS = 1.5V, see the data. At 1.75V, VDS, the device is beginning to have enough power for II to take place. In this operating state, the device's subthreshold slope is measured to be 18mV/dec, which is less than the maximum allowed by CMOS. If the gate voltage from the power source is allowed to continue, the transistors will operate in BJT mode.

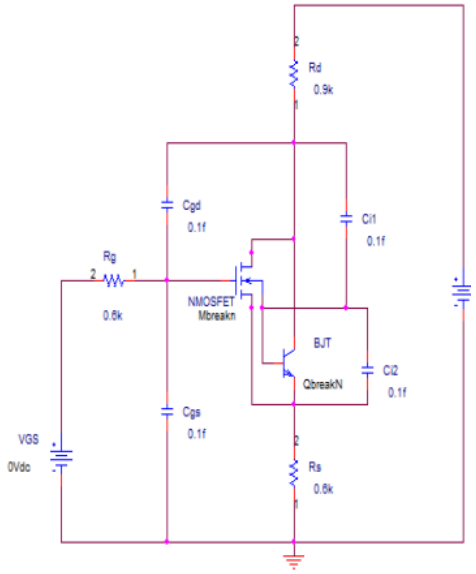

Fig. 5. An equivalent circuit model of vertical IMOS.

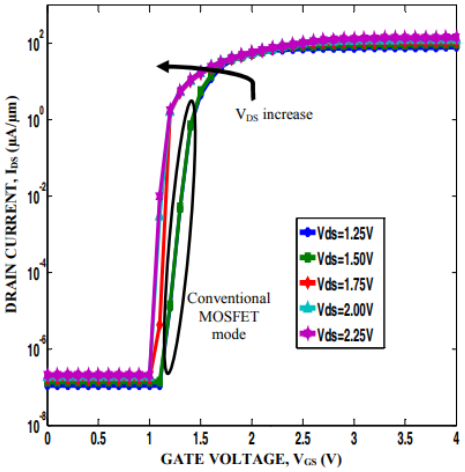

Fig. 6. Transfer Characteristic, IDS vs VGS of the Equivalent Circuit Model for Vertical IMOS

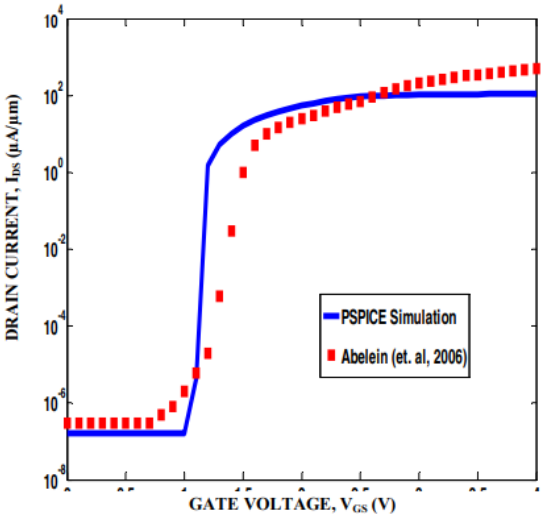

Fig. 7. Comparisons of Transfer Characteristic of the Equivalent Circuit Model with the

Experimental Value of Vertical IMOS at VDS=1.75V

Figure 7 contrasts the PSPICE simulation result with the experimental value found by U. Abelain (2006). When the device is switched on at VDS=1.75V, the ION is 102A/m and the IOFF is 107 A/m, therefore the two values are quite close to one another. Using the circuit equivalent model, we find that the ION/I OFF ratio is 109 A/m, which is larger than the cited experimental value. It is also clear that the subthreshold slope is noticeably shallower than the experimental one. The PSPICE simulation is 90% as close to the experimental result as can be expected. Table 1 provides a tabular representation of the data, allowing for easy comparisons.

Table 1 Comparisons between the equivalent circuit model and the referred experimental value

	Equivalent Circuit Model	U. Abelein (et al, 2006)
S (mV/dec)	18	20
ION (µA/µm)	102	102
IOFF (µA/µm)	10-7	10-6
ION/ IOFF ratio	109	108

5. CONCLUSION

It has been looked at how DG-MOSFETs may be used to create one-of-a-kind low-power current mode analog circuit blocks. We have shown the feasibility of designing and testing current mode analog circuits with customizable performance metrics using the bottom-gate of individually driven DG-MOSFETs using mixed-modal (device + circuit) TCAD simulations. For each kind of tunable current device—a tunable simple current mirror, tunable low voltage cascade current mirror, tunable current amplifier, and tunable current integrator—we have supplied specific examples. Nano-scale DG-MOSFETs have the potential to usher in an age of more efficient, tolerant, and compact circuits with customizable properties, as shown by the circuits and biasing techniques investigated here.

There was a proposal made for a circuit equivalent model of Vertical IMOS, and that model was then studied alongside prior work in order to verify its validity. In addition, the 'Near A valance and Snapback Breakdown' mechanism underlies the resulting circuit. In addition, ORCAD PSPICE was used for analysis of the findings acquired from the device modeling of the Vertical IMOS. The device's ability to extract parameters might lead to novel equation sets. The modeling of the device demonstrates that the experimental values by U. Abelein (2006) and the data reported here are quite close in value. PSPICE simulation's subthreshold slope value is 90% equal to the reference value, according to performance analysis. It is further shown that the PSPICE simulation yields an ION/ IOFF ratio that is just marginally higher than the reference experimental measurement. Therefore, vertical IMOS circuit simulations may be employed, and the vertical IMOS transistor requires further research for biosensor applications.

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Corresponding Author

Ritu Kaundilya*

Research Scholar, A.N. College Boring road Patna India