Design and Calculation of Op-amp using 0.35 micron technology

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Abstract: In this paper to describe the design of a CMOS operational amplifier, which is designed to meet certain given specifications. Based on a clear understanding of the specs, the circuit topology of the standard CMOS operational amplifier was chosen because it was believed that such a design could meet the specs and that the design of such an amplifier is fairly simple. Comparison is drawn between given specifications and result from computer simulations using mentor graphics in the schematic level. Here we had taken 0.35um model from AMS. The results are noted to be satisfactory.

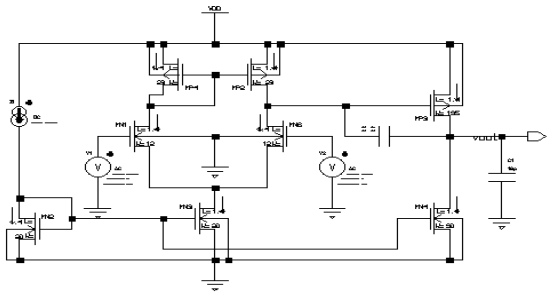
Keywords: *CMOS analog integrated circuit, frequency compensation, operational amplifier, poles and zeros.*

1.1 Deign Procedure for Two-Stage CMOS Op-amp

In designing an op-amp, numerous electrical characteristics, e.g., gain-band width, slew rate, common-mode range, output swing, offset, all have to be taken into consideration. Furthermore, since op-amps are designed to be operated with negative-feedback connection, frequency compensation is necessary for closed-loop stability. Unfortunately, in order to achieve the required degree of stability, generally indicated by phase margin, other performance parameters are usually compromised. As a result, designing an op-amp that meets all specifications needs a good compensation strategy and design methodology. The simplest frequency compensation technique employs the Miller effect by connecting a compensation capacitor, the high-gain state. A Design procedure for this type of op-amp can be found in. However, due to an unintentional feed forward path through the Miller capacitor, a right-half-plane (RHP) zero is also created and the phase margin is degraded. Such a zero, however, can be removed if a proper nullifying resistor is inserted in series with the Miller capacitor..

1.1.1 Topology

The two-stage CMOS op-amp shown in Fig. 1.1 is widely used because of its simple structure and robustness. The best topology for an Op-Amp is



highly dependent on the desired Performance. The Op-Amp DC gain must be greater than 60 dB, settle to 0.1% accuracy is less

Fig 1.1 Schematic of an unbuffered, two-stage CMOS op amp with an n-channel input pair

Figure1.1 shows the topology chosen for this Op-Amp design. This 2-stage, fully differential amplifier consists of a first stage followed by a common-source second stage. The common source second stage increases the DC gain by an order of magnitude and maximizes the output signal swing for a given voltage supply. This is important in reducing the power consumption. Switched-capacitor common-mode feedback was employed to stabilize the common-mode output voltage. The following sections outline a design method for this op-amp topology once the specifications of settling time, gain, noise, and offset are given.

1.1.2 Specifications

1. Gain $\geq$ 70db
2. Gain bandwidth = 10MHz
3. Settling time = 1u sec
4. Slew rate = 10V/usec
5. Input common-mode range, ICMR = 1.5 – 2.8V
6. Common-mode rejection ratio, CMRR $\geq$ 60 db
7. Output-voltage swing = 1- 2.8V

8. Offset ≤ 10 m
9. Layout area= 20,000 square micron

1.1.3 Basic Equetions

Important relationships describing op-amp performance are:

$gm_1 = gm_2 = gmI$, $gm_6 = gmII$, $gds_2 + gds_4 = GI$, and $gds_6 + gds_7 = GII$

$$Id = \frac{Un,p\ Cox(W/L)\ Veff^2}{2} \quad (1)$$

$$gm = \sqrt{2\ Un,p\ Cox\ W/L\ Id} \quad (2)$$

$$gm = 2\ \frac{Id}{Veff} \quad (3)$$

$$\text{Slew Rate SR} = \frac{I_5}{Cc} \quad (4)$$

$$\text{First stage gain } Av_1 = \frac{gm_1}{gds_2 + gds_4} = \frac{2gm_1}{I_5(\lambda_2 + \lambda_4)} \quad (5)$$

$$\text{Second stage gain } Av_2 = \frac{gm_6}{gds_6 + gds_7} = \frac{gm_6}{I_6(\lambda_6 + \lambda_7)} \quad (6)$$

$$\text{Gain Bandwidth } GB = \frac{gm_1}{Cc} \quad (7)$$

$$\text{Outpole pole } p_2 = -\frac{gm_6}{C_L} \quad (8)$$

$$\text{RHP zero } z_1 = \frac{gm_6}{Cc} \quad (9)$$

$$\text{Positive CMR } Vin(max) = VDD - \frac{\sqrt{I_5}}{\sqrt{\beta}} - V_{T03}(max) + V_{T1}(min) \quad (10)$$

$$Negative\ CMR\ Vin(min) = VSS + \frac{\sqrt{I_5}}{\sqrt{\beta}} + V_{T1}(max) + V_{DS5}(sat) \quad (11)$$

$$\text{Saturation voltage } V_{DS(sat)} = \frac{\sqrt{2I_{DS}}}{\sqrt{\beta}} \qquad (12)$$

It is assumed that all transistors are in saturation for the above relationships.

1.1.4 Design Steps

1. The first step is to design the compensation capacitor Cc. Placing the loading pole P_2 2.2 times higher than the GB permitted a 60° phase margin (assuming that the RHP zero z1 is placed at or beyond ten times GB). This results in the following requirement for the minimum value for Cc.

$$Cc > (2.2/10)\, C_L > 0.22 * 10 \text{ pf} \approx 3\text{pf}$$

2. Next, determine the minimum value for the tail current I_5, based upon slew-rate requirements.

The value for I_5 is to be

$$I_5 = SR\ Cc$$
$$= 10 * 10^6 * 3 * 10^{-12}$$
$$= 30 \text{ uA}$$

If the slew-rate specification is not given, then one can choose a value based upon settling time requirements. Determine a value that is roughly ten times faster than the settling-time specification, assuming that the output slews approximately one-half of the supply rail.

3. The aspect ratio of M_3 can now be determined by using the requirement for positive input common-mode range.

$$S_3 = (W/L)_3 = \frac{I_5}{(K'_3)\,[V_{DD} - V_{in}(\max) - |V_{T03}|(\max) + V_{T1}(\min)]^2}$$

$$(W/L)3 = \frac{30 * 10^{-6}}{55 * 10^{-6}\,(3.3 - 2.8 - 0.7827 + 0.467)^2}$$

$$(W/L)3 = (W/L)4 \approx 16$$

If the value determined for $(W/L)_3$ is less than one, then it should be increased to a value that minimizes the product of W and L. This minimizes the area of the gate region, which in turn reduces the gate capacitance. This gate capacitance will affect a pole-zero pair, which causes a small degradation in phase margin.

4. The transconductance of the input transistors can be determined from knowledge of Cc and GB. The transconductance g_{m1} can be calculated using the following equation:

$$g_{m1} = GB\,(Cc)$$
$$= 2 * 3.14 * 10 * 10^6 * 3 * 10^{-12}$$
$$= 188.4\ 10^{-6}$$

5. The aspect ratio (W/L)1 is directly obtainable from g_{m1} as shown below

$$S_1 = (W/L)_1 = \frac{g_{m1}^2}{(K'_2)(I_5)}$$

$$(W/L)1 = \frac{(188.4 * 10^{-6})^2}{156 * 10^{-6} * 30 * 10^{-6}}$$

$$(W/L)1 = (W/L)2 \approx 8$$

6. Now calculate the saturation voltage of transistor M5. Using the negative ICMR equation, calculate V_{DS5}.

$$V_{DS5} = V_{in}(\min) - V_{SS} - \left(\frac{I_5}{\beta_1}\right)^{1/2} - V_{T1}(\max)$$

$$= 0.95 - 0 - \frac{\sqrt{(30 * 10\text{-}6)}}{\sqrt{(156 * 10\text{-}6 * 8)}} - 0.631$$

$$= 0.16395\ V$$

7. Now determine the $(W/L)_5$ using V_{DS5}

$$S_5 = (W/L)_5 = \frac{2(I_5)}{K'_5(V_{DS5})^2}$$

$$(W/L)5 = \frac{2 * 30 * 10^{-6}}{156 * 0.16395^2 * 10^{-6}}$$

$$(W/L)5 \approx 14$$

8. For a phase margin of 60°, the location of the loading pole is assumed to

be placed at 2.2 times GB. Based upon this assumption and the relationship for $|p_2|$, the transconductance gm_6 can be determined using the following relationship

$$g_{m6} > 2.2(gm_2)(C_L/Cc) > \frac{2.2 * 10 * 10^{-12} * 188.4 * 10^{-6}}{3 * 10^{-12}}$$

$$gm_6 = 1381.6 * 10^{-6}$$

9. Since S_3 is known as well as g_{m6} and g_{m3}, (W/L)6 can be calculate using balance conditions,

$$S_6 = S_3\left(\frac{g_{m6}}{g_{m3}}\right)$$

$$(W/L) = \frac{1381.6 * 10^{-6}}{55 * 10^{-6} * 0.2}$$

$$(W/L)_6 = 101$$

10. I_6 can be calculated from the consideration of the "proper mirroring" of first-stage, For accurate current mirroring, V_{SD3} to be equal to V_{SD4}. This will occur if V_{SG4} is equal toV_{SG6}. V_{SG4} will be equal to V_{SG6} if

$$I_6 = \frac{(W/L)_6}{(W/L)_4} I_1 = \left(\frac{S_6}{S_4}\right) I_1$$

$$I_6 = \frac{126 * 15 * 10^{-6}}{I_6}$$

11. The devIce size of M_7 can be determined from the balance equation given below

$$S_7 = (W/L)_7 = (W/L)_5\left(\frac{I_6}{I_5}\right) = S_5\left(\frac{I_6}{I_5}\right)$$

$$(W/L)7 = \frac{14 * 137.72 * 10^{-6}}{30 * 10^{-6}}$$

$$(W/L)7 = 64$$

The first-cut designs of all W/L ratios are now complete.

The total amplifier gain is

$$A_v = \frac{(2)(g_{m2})(g_{m6})}{I_5(\lambda_2 + \lambda_3)I_6(\lambda_6 + \lambda_7)}$$

1.2 Miller Compensation of Two Stage Op-Amp

This technique is applied by connecting a capacitor from the output to the input of the second transconductance stage g_{mII}. The resulting small signal model is illustrated in Fig 1.2(b). Two results come from adding the compensation capacitor Cc. First, the effective capacitance shunting R1 is increased by the additive amount of approximately $g_{mII}(R_{II})(Cc)$. This moves p_1 (the new location of p'_1) closer to the origin of the complex frequency plane by a significant amount (assuming that second stage gain is large). Second, p_2 (the new location of p'_2) is moved from the origin of the complex frequency plane, resulting from the negative feedback reducing the output resistance of the second stage.

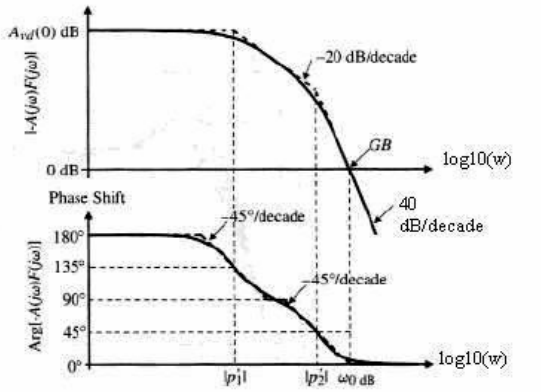


Fig 1.2(a) The open loop frequency response of a negative-feedback loop using an uncompensated op amp and a feedback factor of F(s) = 1

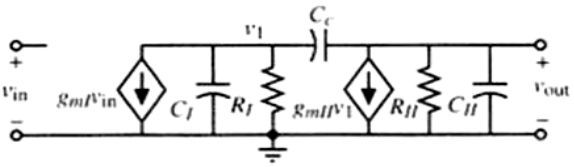


Fig 1.2(b) Miller capacitance applied to the two-stage op-amp

The overall transfer function that results from the addition of Cc is

$$\frac{V_o(s)}{V_{in}(s)} = \frac{(g_{mI})(g_{mII})(R_I)(R_{II})(1 - sC_c/g_{mII})}{1 + s[R_I(C_I + C_c) + R_{II}(C_{II} + C_c) + g_{mII}R_IR_{II}C_c] + s^2R_IR_{II}[C_IC_{II} + C_cC_I + C_cC_{II}]}$$

Two widely spaced poles are given by

$$p_1 \approx \frac{\quad}{-1}$$

$g_{mII}R_IR_{II}Cc$

$$p_2 \cong \frac{-g_{mII}C_c}{C_IC_{II} + C_{II}C_c + C_IC_c}$$

If C_{II} is much greater than C_I and Cc is greater than C_I, then p2 can be approximated by

$$p_2 \approx -\frac{gmII}{C_{II}}$$

It is of interest to note that a zero occurs on the positive-real axis of the complex frequency plane and due to the feedforward path through Cc. The right half-plane zero is located at

$$z_1 = \frac{gmII}{Cc}$$

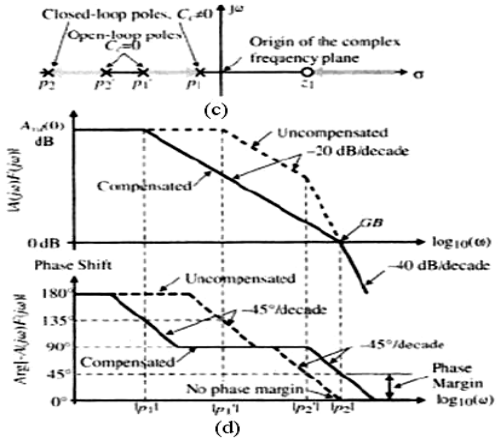


Fig 1.2 (c) & (d)

Fig 1.2 (c) illustrates the movement of the poles from their uncompensated to their compensated positions on the complex frequency plane. Fig.1.2(d)shows results of the compensation illustrated by an asymptotic magnitude and phase plot.

Note that the second pole does not begin to affect the magnitude until after $|A(j\omega)F(j\omega)|$ is less than unity. The right half-plane (RHP) zero increases the phase shift (acts like a left half –plane(LHP) pole) but increases the magnitude(acts like an LHP zero).The task in compensating an amplifier for

closed loop applications is to move all poles and zeros , except for the dominant pole (p_1),, sufficiently away from the origin of the complex frequency plane (beyond the unity gain bandwidth frequency) to result in a phase shift similar to Fig 1.3

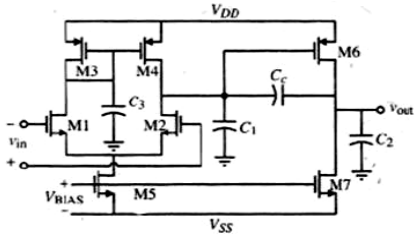


Fig 1.3 Two-stage op amp with various parasitic and circuit capacitances

The approximate pole and zero locations resulting from these capacitances are given below:

$$p_1 \cong \frac{-G_I G_{II}}{g_{mII} C_c} = \frac{-(g_{ds2} + g_{ds4})(g_{ds6} + g_{ds7})}{g_{m6} C_c}$$

$$p_2 \approx - \frac{gmII}{C_{II}} = - \frac{gm6}{C_2}$$

$$z_1 \approx \frac{gmII}{Cc} = \frac{gm6}{Cc}$$

The unity gain bandwidth is shown approximately as

$$GB \approx \frac{gm1}{Cc} = \frac{gm2}{Cc}$$

The above three roots are very important to the dynamic performance of the two-stage Op amp. The dominant left half plane pole p_1, called the *Miller pole* and accomplishes the desired compensation.

1. First Root :

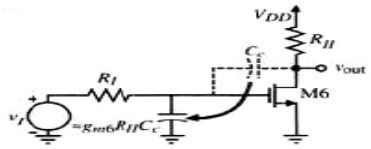


Fig 1.4 Illustration of the implementation of the dominant pole through the Miller effect on Cc. M6 is treated as an NMOS for this illustration.

The capacitor Cc is multiplied by the gain of the second stage, $g_{II}R_{II}$, to give

a capacitor in parallel with R_I of $g_{II}R_{II}Cc$. Multiplying this capacitance times R_I and inverting gives equation of p_1.

2. Second Root :

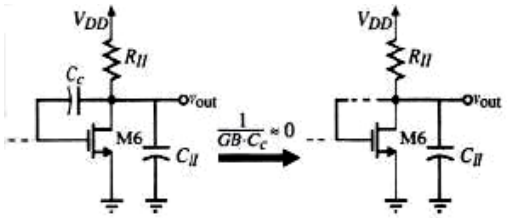


Fig 1.5 Illustration of how the output pole in a two-stage op amp is created. M6 is treated as an NMOS for this illustration.

The second root of importance is p_2. The magnitude of this root must be at least equal to GB and is due to the capacitance at the output of the op amp. It is often called the output pole. Generally, C_{II} is equal to the load capacitance.

Since $|p_2|$ is near or greater than GB, the reactance of Cc is approximately 1/ (GB*Cc) and is very small. For all practical purposes the drain of M6 is connected to the gate of M6 , forming a MOS diode. We know the small signal resistance of a MOS device is $1/g_m$. Multiplying $1/g_m$ by C_{II} (or C_L) and inverting gives equation of p_2.

3. Third Root :

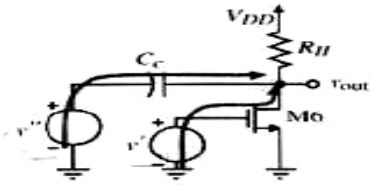


Fig 1.6 Illustration of how the RHP zero is developed. M6 is treated as an NMOS

The third root is the RHP zero. This is a very undesirable root because it boosts the loop gain magnitude while causing the loop phase shift to become more negative. This zero comes from the fact that there are two signal paths from the input to the output as illustrated in Fig. 1.6. One path is from the gate of the M6 through the compensation capacitor, Cc, to the output (V'' to Vout). The other path is through the transistor M6 to the output (V'' to Vout). At some complex frequency, the signals through these two paths will be equal and opposite and cancel, creating the zero. The RHP zero is

developed by using superposition on these two paths as shown below,

$$V_{out}(s) = \left(\frac{-g_{m6}R_{II}(1/sC_c)}{R_{II} + 1/sC_c}\right)V' + \left(\frac{R_{II}}{R_{II} + 1/sC_c}\right)V'' = \frac{-R_{II}(g_{m6}/sC_c - 1)}{R_{II} + 1/sC_c}V$$

Where V = V'= V''

If the zero is placed at least 10 times higher than GB, then in order to achieve 45° Phase margin, the second pole (p_2) must be placed at least 1.22 times higher than GB. In order to obtain 60° of phase margin, p_2 must be placed about 2.2 times higher than GB.

1.3 Location of the Output Pole for a Phase Margin of 60°

For an op-amp model with two poles and one zero, if the zero is ten times higher than GB, then in order to achieve a 60° phase margin, the second pole must be placed at least 2.2 times higher than GB.

The requirement for a 60°phase margin is given as

$$\Phi_M = \pm 180^\circ - \text{Arg}\,[A(j\omega)F(j\omega)]$$
$$= \pm 180^\circ - \tan^{-1}(\omega/|p1|) - \tan^{-1}(\omega/|p2|) - \tan^{-1}(\omega/|z1|)$$
$$= 60^\circ$$

Assuming that the unity-gain frequency is GB, we replace w by GB to get

$$120^\circ = \tan^{-1}\left(\frac{GB}{|p_1|}\right) + \tan^{-1}\left(\frac{GB}{|p_2|}\right) + \tan^{-1}\left(\frac{GB}{z_1}\right) = \tan^{-1}|A_v(0)| + \tan^{-1}\left(\frac{GB}{|p_2|}\right) + \tan^{-1}(0.1)$$

Assuming that Av(0) is large, then the above equation can be reduced to

$$24.30 \approx \tan\text{-}1\left(\frac{GB}{|p_2|}\right)$$

which gives $|p_2| \geq 2.2GB$.

Assuming that a 60 phase margin is required, the following relationships apply

$$\frac{gm_6}{Cc} > 10\,\frac{gm_2}{Cc}$$

Therefore

$$gm_6 > 10gm_2 \quad (13)$$

Furthermore,

$$\frac{gm_6}{C_2} > 2.2\,\frac{gm_2}{Cc} \quad (14)$$

Combining Equation (13) and Equation (14) gives the following requirement:

$$Cc > 2.2\,\frac{C_2}{10} = 0.22C_2 \quad (15)$$

It is proved that in order to achieve a 60° phase margin, the second pole must be placed at least 2.2 times higher than GB.

1.4 Simulation Results

Design parameters of the Op-amp designed by my pro-posed design steps, complete with robust bias part, is shown. ELDO-SPICE simulation results of such an Op-amp under a variety of process conditions and parameters

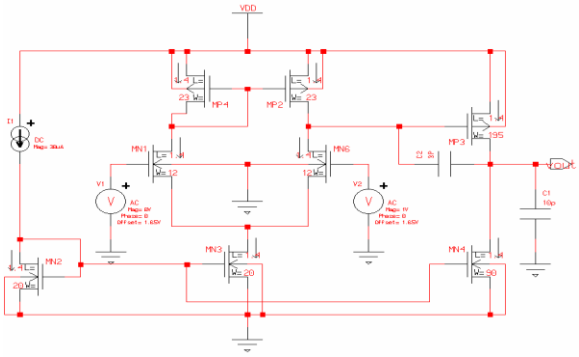
1.4.1 AC Analysis:

In AC- Analysis we determine Phase margin, Gain and GB of the OP-Amp. Both Gain and Phase margin are calculated using DC operating point and AC analysis

Setup:

For determining Gain, DC source with magnitude equal to Vdd/2 to the inverting terminal and apply an AC source with ac magnitude equal to 1 and a dc supply of Vdd/2 to the non inverting terminal is applied. For the gain calculation the two input signals must be different from each other. The magnitude of each input signal should be within the ICMR range (Vdd/2). The setup for AC-Analysis for gain calculation is shown below.
The values given to implement AC-Analysis are

- Start frequency = 1Hz



- Stop frequency = 10 MHz

Fig. 1.7 setup for AC Analysis

Fig 1.8 Output of AC Analysis

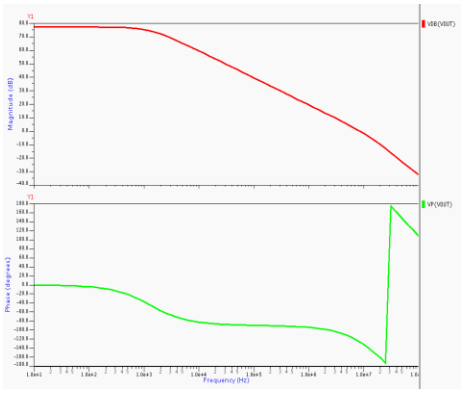
The output results of AC Analysis is as follows

Gain = 77.24 dB

Phase margin = 53.46□.

ω_{-3db} = 1.3 KHz

ω_{UGB} = 8.6 MHz



CMRR= 80.985 dB

To Improve Phase Margin:

To Improve phase margin we use nulling Resistor. The Setup for improved phase margin is shown in figure 1.9.

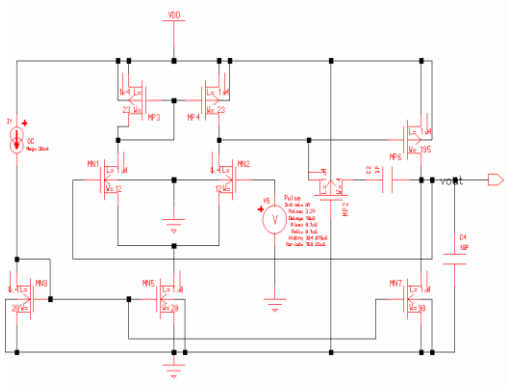


Fig.1.9 Setup for improved phase margin

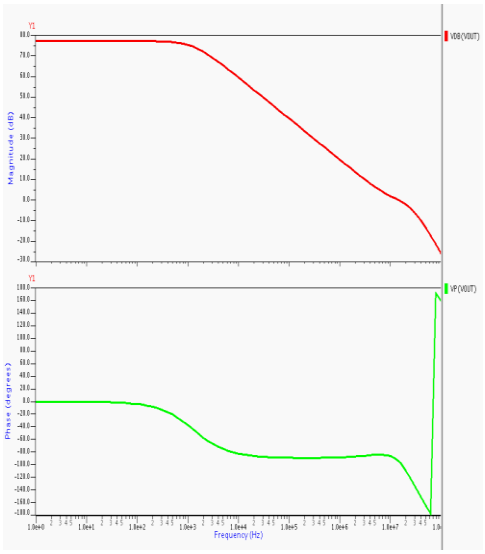


Fig.1.10 Result of AC Analysis

The output results of AC Analysis is as follows
Gain = 77.249 dB
Phase margin = 85.85□
ω_{-3db} = 1.3 KHz
ω_{UGB} = 14.1MHz

CMRR:

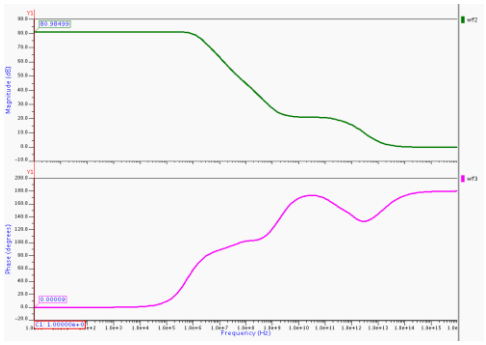


Fig.1.11 Result of CMRR

CMRR = 80.985 dB

1.4.2 Transient analysis

Transient analysis provides information on how circuit elements vary with time. In this analysis inverting terminal of the input and output are shorted and connected to a load capacitance. And the non inverting terminal is connected to a pulse with a rise and fall time equal to one nano second (0.1us) and a pulse width of 384.61us. The values of pulse period is 769.23us. This analysis helps to determine the slew rate of the op-amp.

Slew rate is calculated using the transient analysis. Slew rate is the change of output voltage with respect to time. Typically slew rate is expressed in V/µs. Ideal value of Slew rate is infinite. The slew rate achieved in this design is 10.32V/µs.

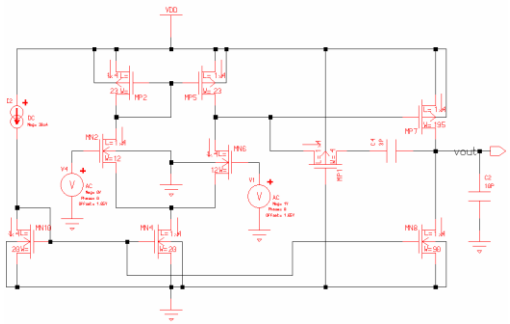
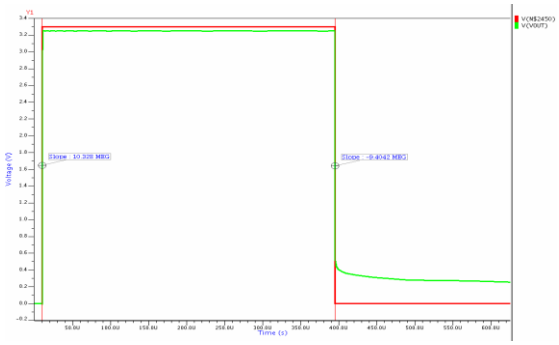
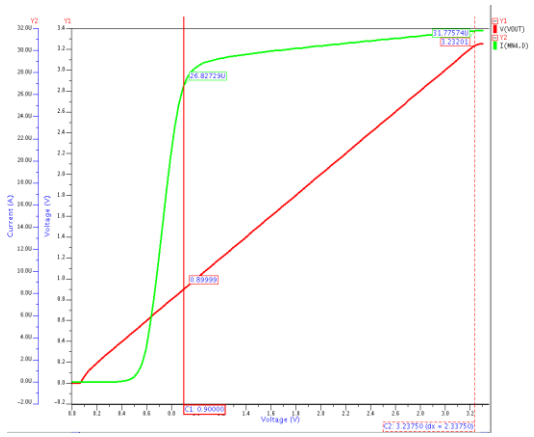


Fig. 1.12 Setup for Transient Analysis



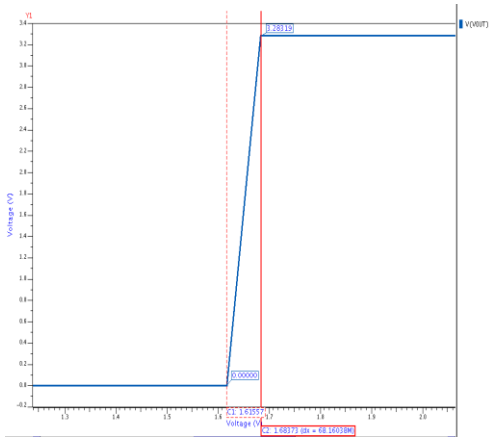
Slew Rate:

Fig. 1.13 Output of Transient Analysis



ICMR:

Fig.1.14 Result of ICMR



Output Swing:

Fig. 1.15 Output Swing

Positive Slew Rate = 10.328V/us
Negative Slew Rate = 9.40V/us
Settling Time = 0.4 us
ICMR = 0.9 – 3.237 V
Output Swing = 0.0 - 3.28V

1.4.3 Scalng:

Reference Circuit L = 1.4 um

Name	Values
W1, W2	12

W3, W4	23
W5, W8	20
W6	195
W7	90

Consider all W/L of reference ckt. as (W/L)1 and f is a multiplication factor.

$$(W/L)n = f * (W/L)1$$

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Biography

Meenakshi Gupta born on November 15, 1983, received his B.Tech (Electronics Communication) from NIET, UPTU, Greater Noida in the year 2005.Her M.Tech. (VLSI Design) from Banasthali Vidyapeeth , Rajasthan in 2008.

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