

# Study of Asynchronous Analog-to-Digital Converter in CAD Graphics

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**Abstract:** This paper contains the asynchronous ADC design specification which has high speed and low power.

**Asynchronous ADC consists of 3 blocks of units composer OPAMP, Digital Logic and Switch Capacitor. Needs high-speed ADC is needed to convert analog signals to digital which is applied to a multimedia device, especially for video signal applications. Low power consumption is useful for efficient power use. The method used in the design is an experiment with simulation CAD software mentor graphics technology with technology CMOS of AMS (Austria Micro Systems) 0.35  $\mu\text{m}$ . Stage design is the A-ADC circuit design with simulation results. The end result is to obtain a design prototype A-3-bits ADC, power consumption <15mW and voltage 3.3 V. CT**

## INTRODUCTION

ADC (Analog to Digital Converter) is one of the main components in digital signal processing systems. As the name implies the ADC is used to convert analog signals (continuous) into digital signal (discrete). Digitizing process done through sampling and quantization. Sampling rate will determine the sample size of unity of time (seconds).

Quantization resolution determines the number of bits that are used to encode the value of each sample. With the continued development of high-speed digital electronic devices that source data is analog data, the role of the ADC continues to rise.

The need for ADC are high now, and must have the following specifications; power consumption and low voltage, has high conversion speed, small delay, and output bits are great. With these specifications Asynchronous ADC is one of the devices that are still widely developed in that direction.

Preparation techniques with unipolar transistors is known as VLSI systems (Very Large Scale Integration) by combining the power engineering and semiconductor companies in the development of a prototype chip VLSI design with CMOS technology (Complementary Metal Oxide Semiconductor, Inc.) for integrated applications (digital equipment) [1,2]. CMOS technology can also be used to design analog and RF circuits CHIP so many complex systems developed with the help of CAD (Computer Aided Design). Development of integrated component technologies

(VLSI) grows progressively smaller size (currently up on 90nm technology) and enabling the development of SOC (System On Chip) for multimedia equipment, eg digital camera, Mobile, Player, Networking and others.

The purpose of this study to obtain the ADC design that has high speed, high accuracy and low power dissipation. In high-speed ADC is typically used to convert the video signal. In this study, expected to be able to design and implement a series of components into the prototype A-3- bits ADC component eg op-amps, comparators, digital logic, DACs (switch capacitor).

## II. ASYNCHRONOUS ADC ARCHITECTURE

Asynchronous sampling ADC and a data type with Nyquis. ADC is a new variant of this type of ADC. When viewed from the way it works is actually a modification of the SAR [5] type ADC. Block diagram of A-ADC, as shown figure 1.

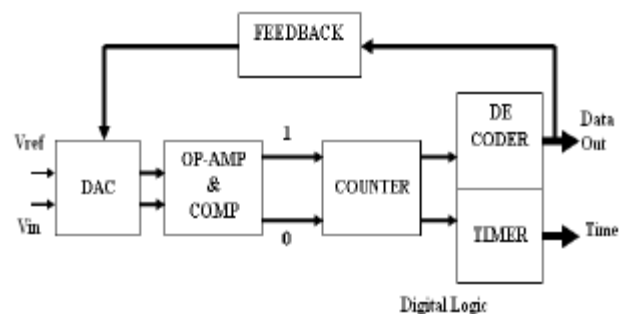


Figure 1. A-ADC Architecture

ADC architecture that is designed in this research is the development of asynchronous ADC architecture (A-ADC), the main design on Switch capacitor [7]. Input analog signals will be captured by the SC to be compared with the signal or reference voltage. In addition to the input signal SC will also get a signal from the decoder which is also a comparison of the digital data signal from the previous signal.

In the figure 1 can see that the signal output from the DAC would go into the OP-AMP and the comparator, which will be processed by these blocks and further into the data '1' and '0' as the driver of the digital logic. Output signal from digital logic block is the data out in the form of digital data and time.

### A. TRANSCONDUCTANCE CMOS OP-AMP (OTA)

The function of the op-amp in the ADC is used to process the sample and hold (SHA) and multiplying, the requirement specifications of the op-amp in the ADC are [2]:

- Gain Open Loop (AoL)  $\geq 2^{N+2}$  V/V (1)
- Gain Open Loop (dB)  $\geq 20 \cdot \log 2^{N+2}$  V/V (2)
- Gain Close Loop (AcL) = 2 V/V (3)
- Freq Unity (fu)  $\geq 0,22(N+1)$  fclock (4)

At figure 2 op-amp OTA circuit, differential amplifier (M1-4) provides two input flip and did not reverse the cause noise and offset. Strengthening (high gam M6-7) is almost similar to the gates of notes when the op-amp drives the low load stage is then followed by a buffer (buffer), flow together (EVI5) are provided by the current mirror circuit [4].

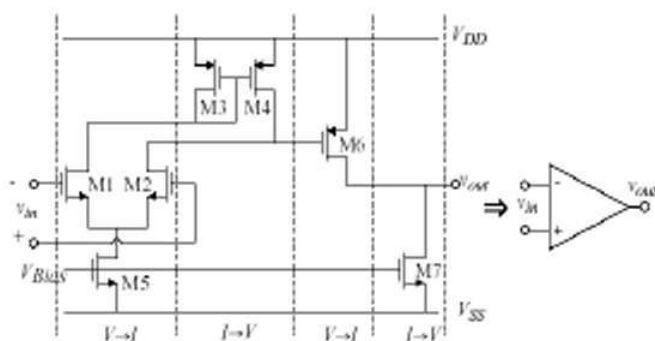


Figure 2. OP-AMP Circuit[6]

Ideal op-amp characteristics, reinforcement of the infinite open mode (AOL = strengthening the closedmode (Buffer = ACL) = 1, infinite input impedance (RIN =  $\infty \Omega$ ), output impedance is almost equal 0 (Ro  $\approx 0 \Omega$ ) strengthening bandwidth (GBW = a large Fout = AV (V +-V-). Av used

with designs on strengthening the open mode (Aol)[2].

All of op-amp has a restriction on its operating voltage range. C'MIR limits (common input mode range) is the border of the scale range of each mput op-amp. outside these limits cause output distortion or truncated.

$$CMR = V_{SS} + \sqrt{\frac{I_{D5}}{\beta_1}} + V_{in(min)} + V_{DSS(max)} \geq 90\% V_{OS} \quad (5)$$

$$CMR = V_{DD} - \sqrt{\frac{I_{D5}}{\beta_3}} - |V_{DS(max)}| + V_{in(max)} \leq 90\% V_{OS} \quad (6)$$

Function of current mirror as bias current source for components for controlling or mos can also drive or as a current mirror with a current source control.

In figure 2 two stage op-amp trans-conductance can be analyzed as follows:

$$I_{D1} = I_{D2} = \frac{I_{SS}}{2}, \text{ slew rate (SR)} = \frac{I_{D5}}{C_c} \quad I_{SS} = I_{D5}, I_{D3} = I_{D4},$$

Gain of stage 1

$$AV1 = \frac{gm_{1,2}}{g_{ds2} + g_{ds4}} = \frac{2gm_{1,2}}{I_{SS}(\lambda_2 + \lambda_4)} \quad (8)$$

Gain of Stage 2

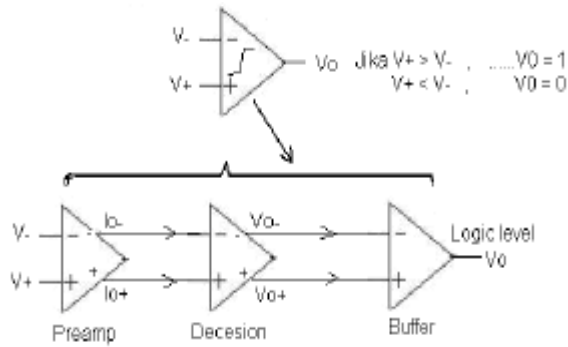
$$AV2 = \frac{gm_6}{g_{ds6} + g_{ds7}} = \frac{gm_6}{I_{D6}(\lambda_6 + \lambda_7)} \quad (9)$$

gds = parameter trans-conductance drain to source

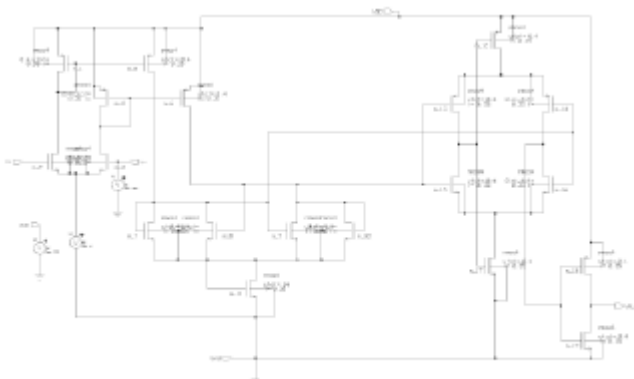
$\lambda$  = parameter channel length modulation

### B. COMPARATOR

The template Function of comparator as input signal comparator with reference tension (ADC), output of comparator is binary logic 0 or 1. at Figure 3 precision comparator block diagram. For unit pre-amp is applied by type differential and in set for capacitance input with active load, unit decision is functioning comparator heart to change from current to tension, Besides as positive feedback by adding component together, applied to shift level hysteresis as well as depressing noise. Prop unit (buffer) functioning as medium level tension to binary logic (0,1).



**Figure 3. Block Diagram Symbols and Precision comparator [4]**



**Figure 4. Comparator Circuit**

Functioning decision unit changes level current to level voltage, hence big of output voltage depended measure M7- M10, and functioning M11 as hysteresis shifter or eliminate noise[4]

If  $I_{o+}$  bigger of value  $I_{o-}$  so M7, M9 to condition ON, and M8, M10 to condition OFF, if value  $\beta_7 = \beta_{10} = \beta_A$  and  $\beta_8 = \beta_9 = \beta_B$  and  $V_{o-} = 0$  so :

$$V_{o+} = \sqrt{\frac{2I_{o+}}{\beta_A}} + V_{THN} \quad (10)$$

$$I_{o-} = \frac{\beta_B}{2} + (V_{o+} - V_{THN})^2 = \frac{\beta_B}{\beta_A} I_{o+} \quad (11)$$

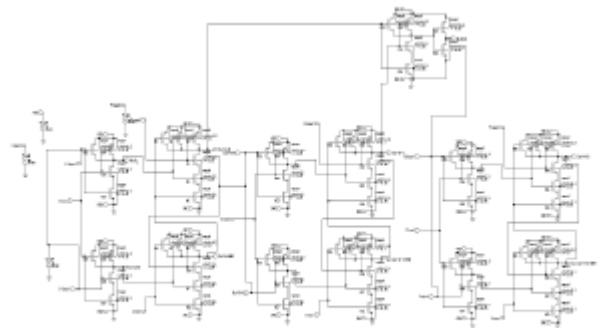
Voltage switching ( $V_{SPH}$ ) :

$$V_{SPH} = V_{o+} - V_{o-} = \frac{I_{SS}}{gm} \cdot \frac{\frac{\beta_B}{\beta_A} - 1}{\frac{\beta_B}{\beta_A} + 1} \text{ for } \beta_B \geq \beta_A \quad (12)$$

### C. DIGITAL LOGIC

Digital logic is a block that serves to process the input signal from the Op-Amp to be used as digital data. This component consists of counters, decoders and timers.

Counter will work based on the input or data from the comparator. When an input '1' it will increase (INC) and if the input '0' then will decrease (DEC). The output of this counter will be two parts, first as a timer and the second as the data out. Out the data size and time depending on the data output of the comparator.



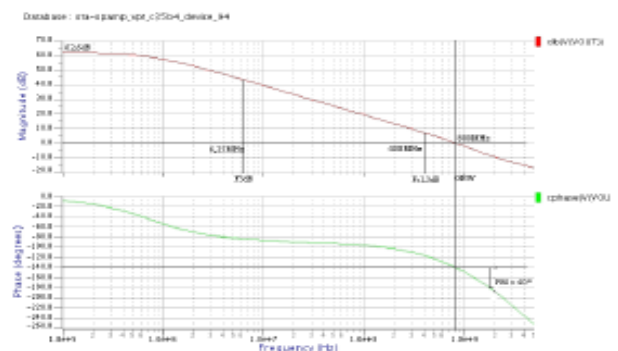
**Figure 5. Counter Circuit**

### D. DAC

DAC is componen for feedback is cooperating with decoder and has errors corection which good for reducing mistake of conversion that is possibly happened. Signal and or this digital data later will be interfaced to DAC to be processed again and becomes perfect digital data.

### III. SIMULATION RESULTS

From the design of each unit can be simulated. The results of each simulation can be described depending on the circuit being simulated. OP-AMP circuits Result simulations like Figure 6.



**Figure 6. Simulation Gain AoL and PM OP-AMP.**

$$AV1 = \frac{gm_{1,2}}{g_{ds2} + g_{ds4}} = \frac{gm_{1,2}}{I_{D2}(\lambda_2 + \lambda_4)}$$

$$AV = 100,35V/V$$

$$AV2 = \frac{gm_6}{g_{ds6} + g_{ds7}} = \frac{gm_6}{I_{D6}(\lambda_6 + \lambda_7)} = 20.89V/V$$

$$AV = 2096,31V/V \text{ (66,42dB)}$$

Calculation of simulation with  $K_n=175\mu A/V$  and  $K_p = 60\mu A/V$ , happened difference with result of simulation equal to 3,62dB if compared to first simulation.

At precision comparator unit (ADC), simulation emphasized at comparator offset

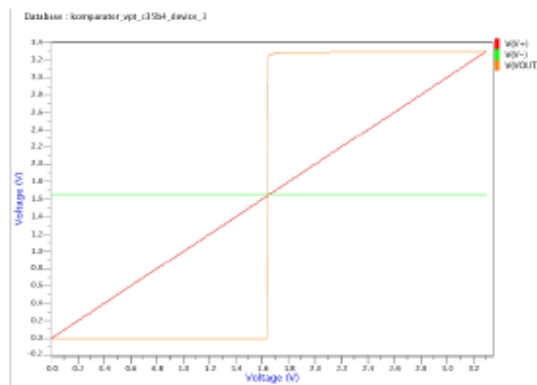


Figure 7. Simulation of Characteristic Vos Comparator

By providing an input DC voltage  $V_{in}$  with a 1.65-V and  $V_{in} +$  variable DC input from 0V to 3.3 V, showed changes in output ( $F_{out}$ ) with set point at 1.65 V. When  $V_{in}$  0V to 1.65V then  $F_{out} = 0V$  (0) and then when  $V_{in}$  moved from 1.65 V to 3.3 V, so  $F_{out} = 3.3 V$  (1) In digital logic units, which are critical to the counter because it blocks all incoming signals and processed at this Counter. The simulation results as Figure 8.

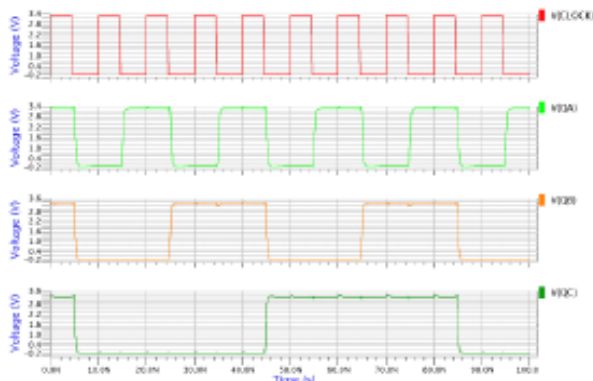


Figure 8. Clock and digital signal

By giving input frequency of 100 MHz can be produced by the counter to count forward or backward according to condition of device.

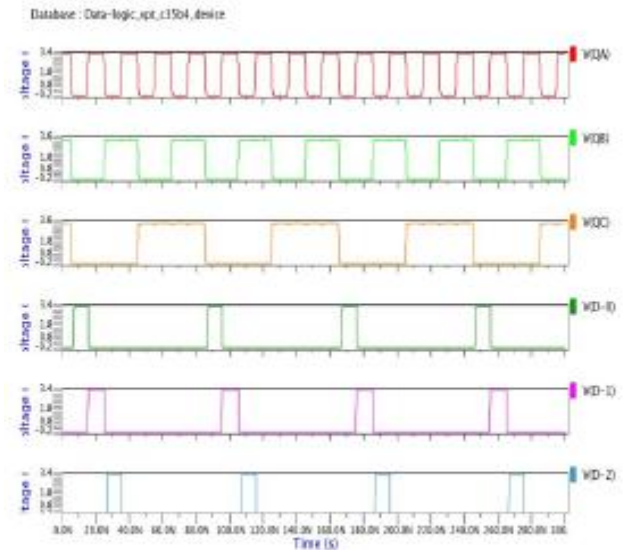


Figure 9. Digital signal and feedback signal

Data out will be converted by decoder and outputs a binary signal will be input to feedback unit, as figure 9. This signals will be a reference to Error Correction .

## IV. CONCLUSION

This Asynchronous ADC has been designed in the schematic (circuit). The result still in the simulation and earns at a speed of frequency 100 MHZ. Application applied for video signal. ADC designed hardly considers resolution and speed that is later can be applied or coupled with equipments of other multimedia or equipments especially for high-speed camera.

## REFERENCES

- [1] B. S. Song, La Jolla, and Gilman," Design CMOS Analog-to-Digital Converter," ECE264C, International WorkShop in University of California, San Diego,2007
- [2] Cheongyuen B.T ,," Digitally Calibrated Analog-to-Digital Converters in Deep Sub-micron CMOS," No.67 UCB/EECS, 22 May 2008.
- [3] E. Allier, J. Goulier, G. Sicard, M. Renaudin, "A 120 nm Low Power Asynchronous ADC", ISLPED 2005

- [4] Eri Prasetyo, Hamzah Afandi, Dominique Gin hac and M. Paindavoine , "A 8-bits Pipeline ADC Design For High Speed Camera Application," IES 2007, ITS 2007
- [5] Eugenio Culurciello, Andreas G. Andreou, " An 8-bit 800-uW 1.23- MS/s Successive Approximation ADC in SOI CMOS", IEEE, Transaction on Circuits and System-II; Vol.53, No.9, September 2006
- [6] J. Baker and D. E. Boyce, " CMOS Circuit Design, Layout and Simulation." IEEE Press on Microelectronic Systems, 1998
- [7] M. Trakimas, S. Sonkusale, Tufts University, "A 0,8 V Asynchronou ADC Energy Constrained Sensing Applications" IEEE, CCIC, pp. 173-176. Januari 2008
- [8] Seung-Chul Lee, Young-Deuk Jeon, and Jong-Kee Kwon, "A 9-Bit 80-MS/s CMOS Pipelined Folding A/D Converter with an Offset Canceling Technique," ETRI Journal, Volume 29, Number 3, June 2007
- [9] Shuo-Wei Michael Chen, Student Member, IEEE, and Robert W. Brodersen, Fellow "A6-bit 600-MS/s 5.3-mW Asynchronous ADC in 0.13-mCMOS" IEEE journal of solid state circuits, vol. 41 no. 12, Desember 2006
- [10] Theja Tulabandhula, Theja Tulabandhula, Yujendra Mitikiri, "A 20MS/s 5.6 mW 6b asynchronous ADC in 0.6um CMOS" IEEE VLSI Design, 22nd, pp. 111-116, 2009
- [11] W. Li, K.L. Shepard, Y. P. Tsividis, "Continuous Time Digital Signal", International Symposium on Asynchronous Circuits and Systems, 2005
- [12] [www.mentor.com/ams.html](http://www.mentor.com/ams.html), 2008 "Parameter Ruler Design CMOS AMS 0,35um," Mentor Graphics Corporation