Study of a Successive Approximation Analog-to-Digital Converter for the Vibration Energy

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Abstract: ***This paper presents a functional design and modeling of a successive approximation analog-to-digital converter (ADC) and its application in the conditioning circuit of the vibration energy harvester. The paper published on BMAS'09 highlighted the necessity of a smart digital control to calibrate the system, which requires in turn an ultra low power supplied ADC. The harvester and the ADC are designed using a CMOS 0.35µm High Voltage technology and modeled in a mixed VHDL-AMS/ELDO environment. The supply voltage of the ADC is 2.5V. The whole system was simulated using a mixed signal Advance MS simulator.***

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1. INTRODUCTION

Modern self-powered autonomous electronic micro-systems, such as wireless micro-sensor network, embedded monitoring systems, biomedical implants, tend to incorporate more functions into smaller surfaces of devices and also are required to operate for a relatively long time without human intervention. On the other hand, the evolution in power source development is not following the same trend: the power supply sources still occupy an important part of size and weight of the system. The energy capacity, as well as lifetime of the existing sources is limited, and alternative energy sources are needed to overcome these bottlenecks.

The autonomy of the devices can be extended by extracting power from ambient energy sources such as light, temperature gradients, mechanical vibration and others. Long lasting, self-renewable, chip-compatible energy harvesting sources are therefore a subject of research for a growing number of scientists and engineers. This study is focused on conversion of the energy of external mechanical vibrations into electrical energy with a use of an electrostatic transducer, which operates as a variable capacitor implemented in a MEMS technology. Harvesting the vibration energy with the capacitive transducer requires complex conditioning electronics for managing the transducer operation and for interfacing the transducer with the load. Harvester, operating under conditions of variable vibration parameters, claims a "smart" power management and adaptive control of the system operation. Our previously published work in BMAS'09 addressed the system adaptation to the variable amplitude of vibrations and, consequently, proposed an adaptive operation algorithm which was implemented in a power management control block and modeled in VHDL - AMS.

The need of measurements of the voltages of the conditioning circuit used for the "smart" control electronics managing the operation of conditioning circuit and the interface with the load requires an analog-to-digital converter with ultra low power consumption. Power saving can be achieved in ADC through the selection of a suitable low-power ADC.

The successive approximation ADC is known as one of the best candidates in terms of low-power. This paper presents the design of a successive approximation ADC, and its modeling in the context of the conditioning circuit presented in [1]. The most critical blocks for the power consumption of the ADC are described at the electrical net list level (the comparator and the digital-to- analog converter, DAC), and the control unit is described behaviorally in VHDL-AMS language. The main goal of the mixed modeling of the whole system (ADC+conditioning circuit) is an estimation of the power losses associated with the electromechanical power conversion and with the measures of the electrical state of the conditioning circuit needed for the calibration. This estimation doesn't take into account the consumption related with purely digital blocks.

In section 2, we summarize the basic architecture and the operation of the harvester as well as the calibration technique allowing the adaptation of the system to the vibration parameters. In section 3, we present the architecture of the successive approximation ADC and we explain the implementation and modeling approach for each block. In section 4, the connection of harvester system with the ADC, calibration technique is discussed and simulation results of the whole system are shown.

2. SUCCESSIVE APPROXIMATION ADC ARCHITECTURE

In Fig. 2, we can see how different parts of the successive approximation ADC are connected. In our topology, the signal is sampled in the first clock cycle and is converted in the next N clock cycles, where N is the number of bits. The sample and hold operation is achieved with the use of the DAC, when it is set in"sampling" mode. The DAC, allowing to achieve the successive approximation of the input voltage value, contains an array of binary weighted capacitors whose topology can be reconfigured by switches. The DAC output is connected to the negative input terminal of the comparator as it is shown in Fig. 3, while the common mode voltage Ucm is connected to the positive input terminal and the comparator output is connected to the control unit. The control unit represents the successive approximation register (SAR) that controls the DAC switches allowing to switch capacitors terminals to the three reference voltages: the supply voltage Udd, the common mode voltage Ucm = Udd/2 and the ground gnd. It generates the output digital word representing the digitally approximated input voltage. This architecture was described in details in [6].

2.1 SUCCESSIVE APPROXIMATION ADC STAGES

This section describes stages of successive approximation ADC conversion, achieved in different modes.

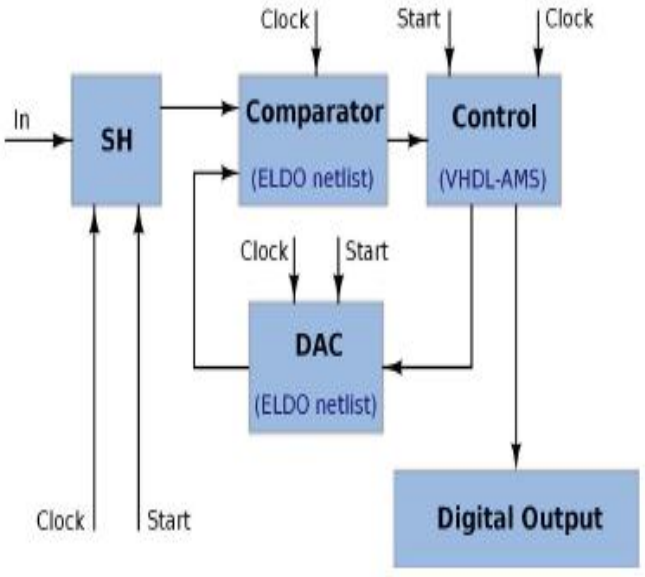

Figure 2: Successive approximation ADC architecture

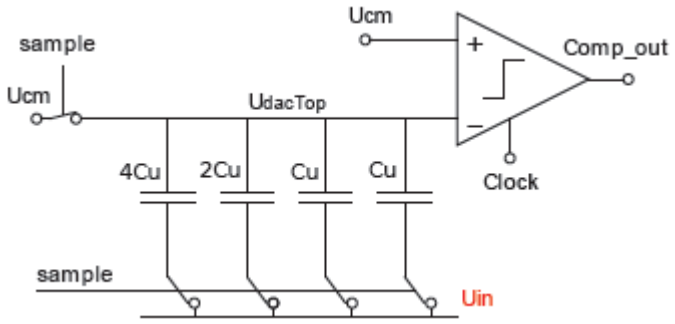

Figure 3: Sampling Mode in successive approximation ADC with 4 bits

In the first half cycle of the first clock cycle, the DAC capacitors bottom plates in the capacitor array are connected to the input signal Uin, while the top plates are connected to Udd/2: this is the "sampling" mode and it corresponds to the configuration shown in Fig. 3. In the second half of the clock cycle, all bottom plates are connected to Udd/2: this is the inversion mode. After the first cycle, the control unit checks the comparator output (comp out). If it is high, it connects the largest capacitor bottom plate to Udd, if it is low, the control unit connects the largest capacitor bottom plate to gnd. This mode is called charge redistribution mode.

The same is repeated with all capacitors in the array, in N clock cycles. At ith clock cycle, the output of the comparator correspond to ith bit of the output ADC word. This bit value is saved by the control unit and after the end of the charge redistribution mode, the digital output of the control unit is equal to the digitally approximated input voltage. In Fig. 4, we can see how the voltage of the DAC top plates changes in every mode on the example of 8-bit successive approximation ADC.

2.2 COMPARATOR CIRCUIT

The comparator in Fig. 5 is designed in CMOS 0.35 µm technology. This is a semi-dynamic clocked architecture and it compares the output of the DAC UDAC Top that is connected to the negative terminal and Ucm that is connected to the positive terminal. Transistors M1 and M2 are used to amplify the input signal. Transistors M3, M4, M9 and M10 implement a couple of inverters connected so to be a flip-flop (back to back inverters). Transistors sizes are chosen with a low aspect ratio so as to reduce the power consumption and with a large area to reduce the offset mismatch. The comparator uses an internal clock equal to 2.5KHz. Thus, using the resolution of the ADC N = 8 bit, the sampling frequency is 277.78 Hz (2.5KHz/N+1), i.e the sampling time step equals to 3.6ms. The average current consumed in one conversion step equals to 0.5µA. As shown in Fig. 6, the comparator

resolution is lower than ULSB = 9.8mV. Both comparator outputs are connected to a latch to keep the comparator output stable for every clock cycle.

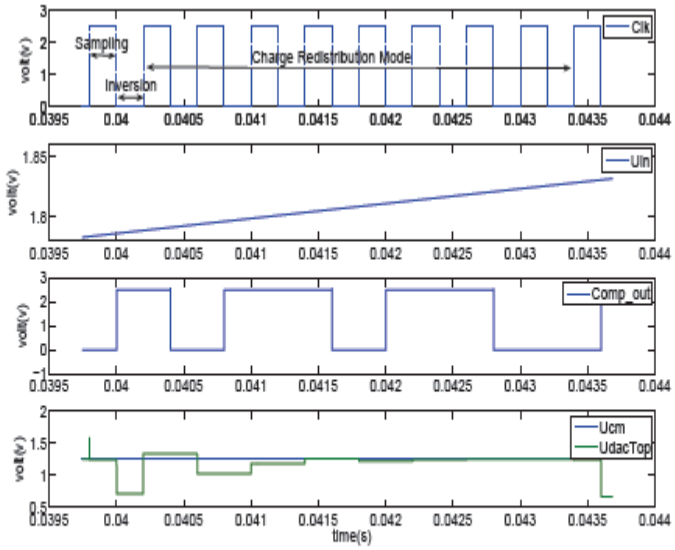

Figure 4: 8-bit successive approximation ADC modes

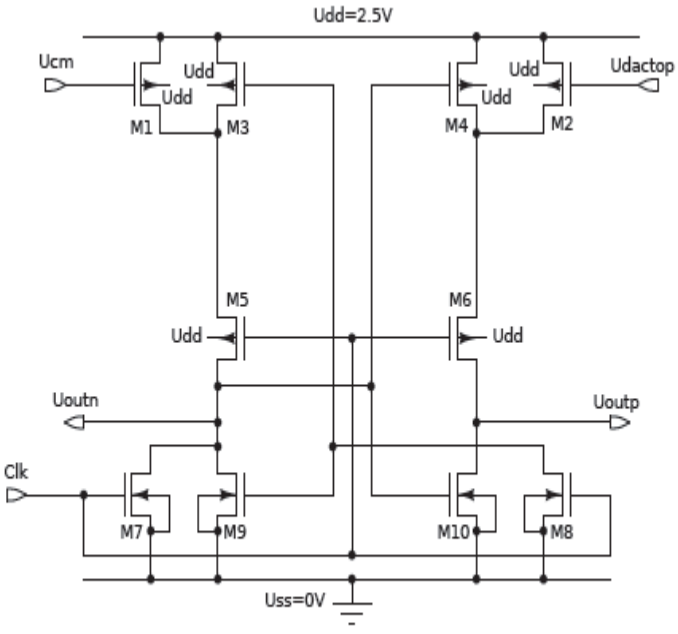

Figure 5: Comparator circuit

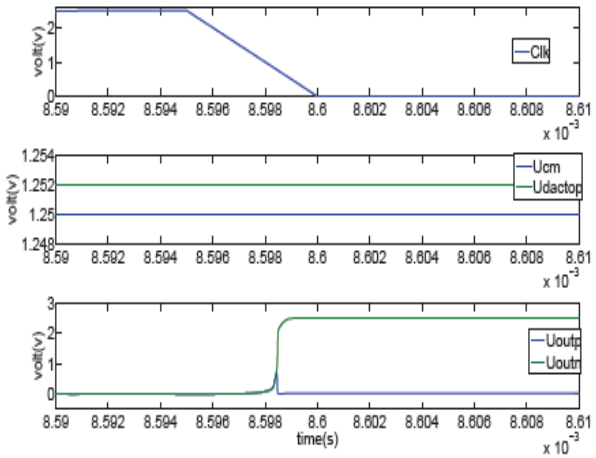

Figure 6: Comparator Resolution

2.3 DIGITAL TO ANALOG CONVERTER CIRCUIT

The DAC is designed in CMOS 0.35 µm technology and it contains 8 binary weighted capacitors in the array, the top plates are connected together. At each bottom plate, there are ideal switches to connect the bottom plate with the input signal and the three references as shown in Fig. 7.

The choice of the unit capacitance value (Cu) depends on the input capacitance of the comparator, the needed resolution and the sampling frequency.

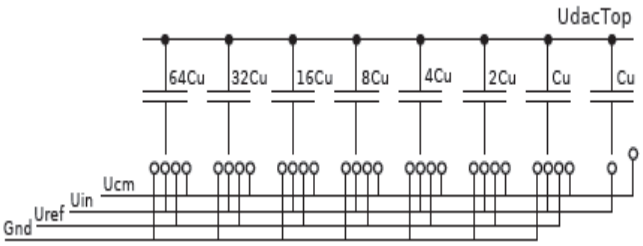

Figure 7: Differential DAC of a 8-bit successive approximation ADC with unit capacitance Cu

2.4 CONTROL UNIT VHDL-AMS MODEL

The output of the comparator is connected to the SAR control unit. At the sampling mode, the SAR control unit commands the switches so that the upper plates of the array are connected to Udd/2 and the bottom plates are connected to Uin. Then, at inversion mode, it commands switches so that the bottom plates are connected to Udd/2. In each clock cycle of the charge redistribution mode, depending on the comparator output, the control unit decides either to connect the corresponding weighted capacitor bottom plate to Udd or to gnd. In this way, the control unit raises or reduces voltages on the top plates of

the capacitors array by binary weighed level voltages (Udd/4, Udd/8,...,Udd/256), so achieving the successive approximation of the input voltage. This block was described in VHDL-AMS language as it is shown in the code below.

```
entity control4  is
 generic(n : integer := 8);
port (
--internal clock:
signal clock: in std_logic;
--sampling clock:
signal start: in std_logic;
--comparator output terminal:
terminal toutp : electrical;
--to control Uref switches
terminal tin01br, tin02br, tin03br,
tin04br, tin05br,
tin06br, tin07br : electrical;
--to control ground switches
terminal tin01bg, tin02bg, tin03bg,
tin04bg, tin05bg,
 tin06bg, tin07bg : electrical;
--to control Ucm switches:
terminal tin01bcm, tin02bcm, tin03bcm,
tin04bcm,tin05bcm, tin06bcm,
tin07bcm, tin08bcmx : electrical;

terminal tgnd : electrical;
-- output bits:
signal dout: out unsigned(7 downto 0)
);
begin
end entity control4;
architecture fct of control4 is
--quantity declaration
--signal declaration
begin
p1: process
variable i :integer :=n ;
variable word : unsigned((n-1)downto 0);
begin
-- disable all control signals
LOOP
wait on clock;
--first cycle in charge redistribution mode
if clock'event and clock='1' and start='0'
and (i=n) then
i:=n-1;
--connect the capacitors
--bottom plates to Ucm
in02bcm<=2.5;
in03bcm<=2.5;
in04bcm<=2.5;
in05bcm<=2.5;
in06bcm<=2.5;
in07bcm<=2.5;
in08bcmx<=2.5;
if (comp_out>1) then
word(i):= '1';--msb=1
in01br<= 2.5;--connect the msb cap to Uref
else
word(i):= '0';--msb=0
in01bg<= 2.5;--connect the msb cap to gnd
end if;
else

--second cycle in charge distribution mode
if clock'event and clock ='1' and start = '0'
and (i=n-1) then
--connect the capacitors bottom plates to Ucm
i:=i-1;
in02bcm<=0.0;
in03bcm<=2.5;
in04bcm<=2.5;
in05bcm<=2.5;
in06bcm<=2.5;
in07bcm<=2.5;
in08bcmx<=2.5;
if (comp_out>1) then
word(i):= '1';-- 2nd bit=1
in02br<= 2.5;--connect the 2nd cap to Uref
else
word(i):= '0';-- 2nd bit=0
in02bg<= 2.5;--connect the 2nd cap to gnd
end if;
else
```

```
-- this algorithm is repeated
-- to i=n-7
--last cycle in charge distribution mode
if clock'event and clock ='1' and start'event
and start='1' and (i=n-7) then
--connect the capacitors
--bottom plates to Ucm
i:=i-1;
in08bcmx<=2.5;
if (comp_out>1) then
word(i):= '1';-- lsb bit=1
else
word(i):= '0';-- lsb bit=0
end if;
-- we get the new output bits
--at the end of the conversion
dout<=word;
i:=n;
--disable all control signals
end loop;
end process;
end architecture fct;
```

3. APPLICATION OF SAR ADC INTO THE HARVESTER CONDITIONINGCIRCUIT

In this section, we present the use of the designed successive approximation ADC in the conditioning circuit of harvester, whose model architecture is shown in Fig. 8. The ADC measures only the Ustore voltage, whereas the value of Ures can be found from the determined value of the Ustore converted voltage as we will explain later in this section. For optimal operation, the harvester requires the high voltage on Cstore, hence, to interface the low-voltage ADC input with the high-voltage Ustore node of the conditioning circuit, a voltage divider is needed. The output bits of the ADC are connected to the flyback switch control input which uses the measured values of Ures and Ustore max to calculate U1 and U2. As soon as U1 and U2 are calculated, the switching events for the switch Sw are generated with the signals on2 or off2, as shown in Fig. 8. The fly back switch control activates the ADC with the signals on1 or off1, so that the ADC operates only during the calibration cycle.

As it is shown in Fig. 8, the whole harvester system model is mixed: it contains VHDL-AMS models of the fly back switch control, the switch, the variable transducer capacitor with the resonator, the VHDL-AMS/ELDO model of the ADC, ELDO models of the voltage divider and of the rest analog components such as capacitors, inductor and diodes. In this

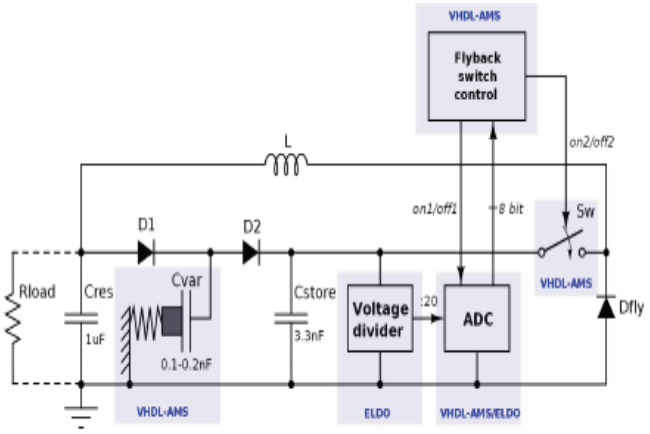

Figure 8: Functional schema of harvester system

section, firstly, we discuss the divider architecture and its operation, then the use of ADC during the calibration cycle and, at last, the whole system simulation results.

3.1 VOLTAGE DIVIDER CIRCUIT

In present work the division factor of divider is 20, since the maximal value for Ustore is limited by 50V and the voltage supplied by the ADC is 2.5V. The proposed divider consists of 2 resistors connecting in series, 2 switches and an output capacitor as shown in Fig. 9. At every sample, resistors divide Ustore by 20, and the divided voltage is stored in the capacitor Cdiv, so that the successive approximation ADC can sample this value. The clock used in the divider (CLK DIV) has the same sampling frequency but with the smaller pulse width to decrease the power consumption. The relation between Ustore and the divider output Uout div can be calculated based on equation:

$$\frac{U_{\text{store}}}{U_{\text{out\_div}}} = \frac{R_1 + R_2}{R_2} = 20 \qquad (3)$$

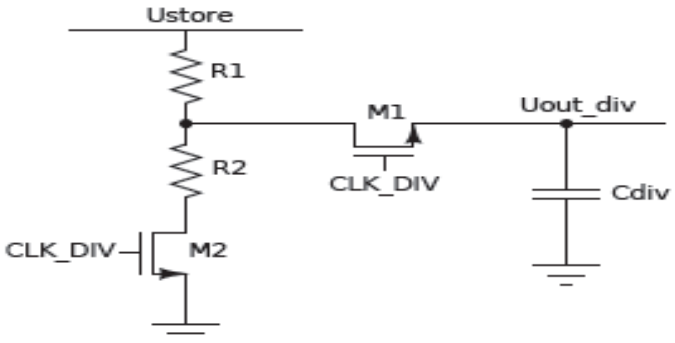

Figure 9: Voltage divider circuit interfacing the harvester with the ADC

Hence, from (3) we have R1 = 19R2. The time of charging Cdiv is determined by:

$$\tau = R_1 \parallel R_2 \cdot C_{\text{div}}, \qquad (4)$$

The presented voltage divider circuit is designed in CMOS 0.35µm high voltage technology of Austrian Microsystem (AMS035HV), and modeled using the ELDO simulator.

3.2 CALIBRATION USING SUCCESSIVE APPROXIMATION ADC

The calibration cycle starts with putting U1 to a very low value (zero), so that Cstore voltage becomes equal to Cres voltage. During 20 ms Ustore remains at the Ures value, which gives to the ADC enough time to measure it. After that, the flyback switch control orders the charge pumping to start, and Ustore starts to increase, up to the saturation.

During this charge pumping, the voltage Ustore is measured with 3.6 ms sampling step. The goal of this measurement is to detect the Ustore max value. This is done as described in the section 2; the digital values corresponding to the neighboring samples of Ustore are compared, and when there are 2 consecutive steps have the same value, their value is considered as measured Ustoremax (it means that _Umin mentioned in section 2 equals to the ADC resolution). At the end of the calibration cycle the flyback switch control block turns off the ADC and U1 as well as U2 are calculated.

Then, the normal mode (periodic charge pump + fly back cycles) starts till the next calibration cycle as it is shown in the Fig. 10.

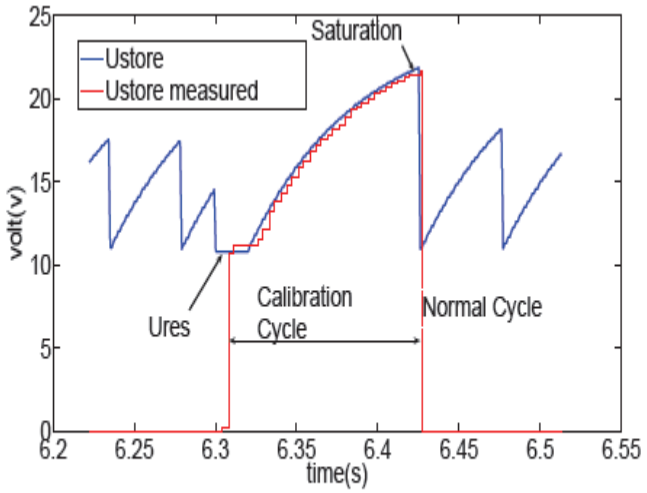

Figure 10: Calibration cycle of the harvester

3.3 MODELING RESULTS

In order to validate our study we created and simulated models of the divider and of the successive approximation ADC and connected them to the conditioning circuit model as it is shown in the Fig. 8. In this paper, we present simulation results which demonstrate the harvester operation with ADC during almost 11 seconds. Here, calibration cycles repeat every 900ms, such a low interval is chosen in order to reduce the modeling time, in reality the calibration phase should be less frequent (tens of seconds) to reduce the power consumed.

In the top part of the Fig. 11, Ustore is plotted together with the measured Ustore voltage. We can see that during the calibration cycle there is a good matching between them because of the good resolution of the ADC. In the bottom part of the Fig. 11, the real Ures is plotted with the measured Ures voltage. The increase in the real Ures value is explained by the accumulation of the energy of the system (i.e., a normal harvester operation). As we see, Ures is measured only once during the calibration cycle. In the normal operation mode between calibration cycles ADC is deactivated by the signal off1. The measured Ustoremax value is reset to 0 and the equivalent Ures is saved until the next calibration cycle.

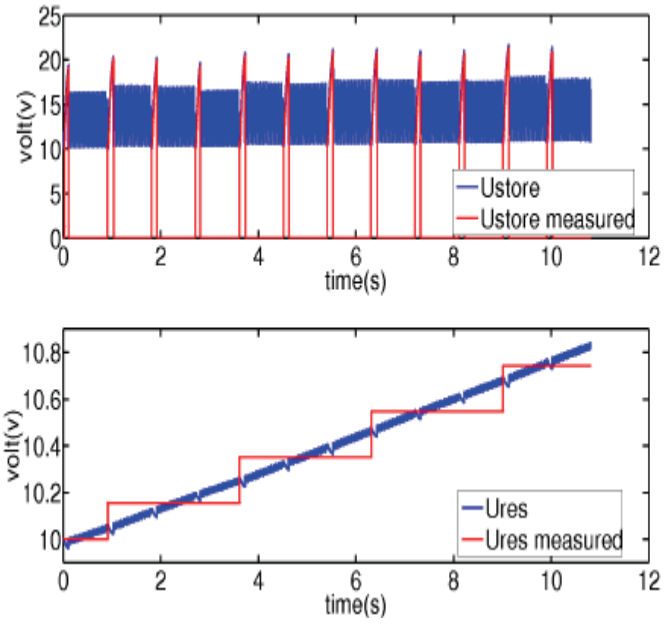

Figure 11: Simulation results of harvester operation using the SAR ADC model

4. CONCLUSIONS

In this paper, we presented the architecture design and modeling of the electrostatic vibration energy harvester with a successive approximation ADC. The use of such

ADC in energy harvester application is suitable for a low power consumption. The whole system of the harvester including the SAR ADC is simulated with VHDL-AMS/ELDO mixed model using the cadence environment. Simulation results of the harvester with the use of 8-bit SAR ADC demonstrate a good matching between Ustore and the measured from ADC Ustoremes during the calibration cycle. The estimated power consumption of the ADC is around 1.25µW for one step conversion. The comparator is the dominating block in power consumption of ADC with the used sampling frequency and 8-bit resolution, whereas the DAC has much less contribution. The modeling approach consisting in mixing the description levels and the disciplines is very efficient; the VHDL-AMS/ELDO mixed modeling appears as the best solution for low-level design of electrical interfaces for energy conversion.

5. REFERENCES

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