

Evolution of Communication Technologies from Sequential to Parallel Computing

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Abstract – This section features the need of logical parallel computing to take care of complex logical issues like Genome sequencing, plan of nuclear bomb, reemergence directions of room vehicles and so forth that interest huge scope calculations. Numerous logical projects are likewise recorded that were started to foster such huge foundation. This prompted the advancement of different models for communication technologies therefore today the calculation rates of logical parallel computers are seen to have outperformed the peta FLOPS mark. The part makes a critical blemish on the Indian commitments to the advancement of communication technologies in logical parallel computing particularly the Floswitch at the Flosolver lab of National Aerospace Laboratories, Bangalore. The part closes with the notice on arising difficulties, new standards and conceivable outcomes in the advancement of the Floswitch.

Keywords – Parallel Computing, Floswitch, Communication Technology

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INTRODUCTION

Development of Computing Technology Large scope computing has assumed significant part in tackling complex logical and mechanical issues. Genome sequencing has been conceivable because of huge scope computational assets (Mark Delderfield et al 2008). The plan of nuclear bomb got attainable just with the assistance of crude PC . New medication improvement regularly utilizes enormous scope computing . Numerous new revelations have been consequence of huge scope calculations. For instance, single waves were found by Ulam and his partners utilizing huge scope computing; space missions request enormous computing for reemergence directions of room vehicles and mathematical exactness surpassing 20 digits are very normal.

It is, in this manner, not astonishing that prerequisite of enormous scope calculations has prompted improvement of parallel machines with history tracing all the way back to 1960's. The account of advancements of the computers being used till mid 70's is all around archived and clearly introduced in the reference which makes an interesting perusing. The fundamental premium here is to get a vibe of the development pace of force of computing. The chart in the Figure 1. is an ordinary figure which is discovered as often as possible in the connected works that schematically shows the historical backdrop of development of computing power since 1950. For additional development it isn't astounding that course

of parallel handling arose in a characteristic manner as the exchanging time and engendering delay were being restricted with the cut-off set by the speed of light.

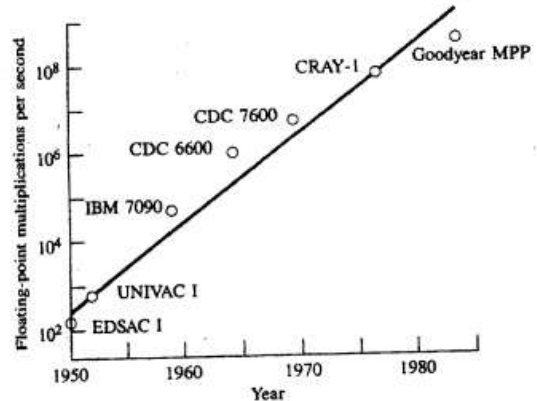


Figure 1 growth rate of computing power

Distinctive Features of Parallel Computing

In parallel handling the undertaking is split between different Processing Elements (PEs) that execute the positions in parallel. It is verifiably expected here that the assignment is agreeable to parallel preparing and communication component is set up so PEs may chip away at the subtasks of the principle task but then complete the fundamental errand as though the cycle is done on a solitary virtual sequential

computing machine. Communication worldview shows up at a go across street now. Communication issues in the prior sequential PC were identified with interconnection of CPU components, for instance in the plan of CDC 7600 it was identified with empowering the CPU for skimming point division in a solitary cycle or in modem times making a super pipeline construction of Pentium for doing a solitary gliding point activity per cycle in a pipeline; though for parallel preparing communication it ordinarily alludes to communication among PEs on a plainly visible or net or at course grained level. Execution of shared memory engineering in equipment is requesting. Infact, it is just about as troublesome as making a pass on for a CPU chip. Moreover, as adaptability issues for such design have remained to a great extent unanswered and if the example of improvement is any sign, it is gotten comfortable the negative. The current overview alludes to the non-shared memory kind of communication issues.

Parallel computing a natural tool for handling large problems of Mathematical Physics

It is an adage that the field conditions happening in science when fittingly detailed are amiable to conveyed parallel handling. A straightforward model will represent the view point. The arrangement of the potential condition which is formed through Green's capacity isn't normally amiable to parallel preparing though when figured by limited contrast discretisation drives normally to area decay procedure which is exceptionally managable to parallel handling The PEs in the parallel machines are accordingly needed to collaborate to tackle a specific undertaking requiring interconnection conspire for speaking with one another. Such climate offers quicker answer for complex issues than attainable utilizing sequential machines. Also sequential machines will be unable to take care of the issue in sensible measure of time. The interconnection network needed for the PEs to impart structures the main piece of a parallel PC close to Central Processing Units (CPUs).

Contemporary Parallel Computers -

Typical Examples i. **Earth Simulator:** The Earth Simulator (ES), created by the Japanese government's drive "Earth Simulator Project", has been a profoundly parallel vector supercomputer framework for running worldwide environment models to assess the impacts of a dangerous atmospheric deviation and issues in strong earth geophysics and other huge scope computing issues. The framework was produced for Japan Aerospace Exploration Agency, Japan Atomic Energy Research Institute, and Japan Marine Science and Technology Center with a pinnacle execution of 35.86 TFLOPS. Worked by NEC, ES depended on their SX-6 design where a solitary chip execution containing a vector processor unit and a scalar processor was created in a 0.15 μm CMOS measure with copper interconnects.

Blue Gene: In September 2004, IBM announced that a Blue Gene/L prototype at IBM Rochester (Minnesota) had overtaken NEC's Earth Simulator as the fastest computer in the world, with a speed of 36.01 TFLOPS on the LINPACK benchmark, beating Earth Simulator's 35.86 TFLOPS. This was achieved with an 8-cabinet system, with each cabinet holding 1,024 computing nodes. Lawrence Livermore National Laboratory (LLNL) and IBM announced that Blue Gene/L had once again broken its speed record, reaching 280.6 TFLOPS, upon reaching its final configuration of 65,536 "compute nodes" (i.e., 216 nodes) and an additional 1024 "I/O nodes" in 64 air-cooled cabinets interconnected using three-dimensional torus interconnect with auxiliary networks for global communications, I/O, and management.

Flosolver: In the Flosolver arrangement, its Mk-8 Parallel Computer being created at National Aerospace Laboratories (NAL) comprising of 1024 processors interconnected utilizing modified communication switch called Floswitch. The Flosolver Mk-8 is required to convey a pinnacle execution of 10 TFLOPS and is principally utilized for taking care of different CFD issues, Weather determining and so on The unmistakable element of this machine is its tweaked Floswitch, which messages preparing related to message passing. It is intended for a vastly improved versatility for firmly coupled class of issues like climate displaying or direct recreation of Navier-Stokes conditions.

Evolution of Communication Technologies from Sequential to Parallel Computing

Sequential Computing Earlier computers were straightforward arithmetical information taking care of machines and were electromechanical in nature. The development of diode, triode and so forth made of vacuum tubes gave a significant forward leap during the time spent creating computing machines, and the electronic computers like ENIAC and so on were trailblazers. UNIVAC, DEC CDC, Burroughs (Gray G T and Smith R Q 2009) and numerous different centralized servers overwhelmed the scene during the 60's and 70's as centralized computer computers. The vacuum tubes were supplanted by semiconductors which offered scaling down, decreased postponements and upgraded dependability. The computational interest had effectively required the thought of vector computing in the mid 70's during which period CDC machines became famous and Japanese machines like NEC Fujitsu and so forth arose as a solid contenders to USA supercomputing industry. The semiconductor further prompted the significant creation of microchips that overwhelm the current day computers.

Development during the mid eighties

The mid 80's was a period of quick advancement in the computational technologies. These

advancements had huge effect in the field of science and related mechanical turn of events. The prerequisites of huge calculations were consistently filling in the always bigger number of uses and the computing power bounced from the request for MFLOPS to GFLOPS and to TFLOPS and afterward to Peta FLOPS. In sequential computing, the communication was restricted to inside the processor and between the registers. With the thought of parallel computing, communication must be set up across the CPU's in a coarse grained or perceptible manner. After the creation of microchip the chance of building parallel computers was seized in everywhere on the world

Growth of Parallel Computing in India

The accomplishment of NAL's parallel computing brought about setting up of CDAC, Center for Development of Advanced Computing in 1988, a public drive on a lot bigger and goal-oriented scale CDAC finished its PARAM parallel PC in July 1991 with a pinnacle execution of 1 GFLOPS. It was a 256-hub framework containing a gathering of 64 hubs organized through computing bunches. These computing groups were interconnected inside and remotely through cross-direct switches toward structure a 256-hub framework. PARAM Yuva being the most recent of the PARAM arrangement of supercomputer created in June 2009. It is equipped for performing at 38.1 TFLOPS. The most recent equipment PARAM net is a fast high data transmission low inertness network created for PARAM arrangement. The first PARAM net uses a 8 port course capable non-obstructing switch created by CDAC. Each port gave 50 Mb/s in (along these lines 2x50 Mbit/s) full-duplex organization and was first utilized in PARAM 10000 (Rajaraman V 1999). PARAM net II, presented with PARAM Padma, is equipped for 2.5 Gb/s while working in full duplex that upholds interfaces like Virtual Interface Architecture and Active Messages. It utilizes 8 or 16 port SAN switches and furthermore frames the reason for the lattice computing network GARUDA (Singh A K 2007). The significant uses of PARAM are in long-range climate gauging, distant detecting, drug plan, atomic displaying and so on.

Indian Contribution to Communication Technology

The Floswitch in Flosolver arrangement of parallel computers has been a result of involvement acquired in planning parallel machines having better versatility highlights for firmly coupled issues. It arose that the worldview of just message communication restricts the presentation. On the off chance that switches were given the additional element of message preparing, the adaptability could be essentially improved. This was the beginning of Floswitch. At the end of the day, this worldview of communication switch measures data while conveying and it brings about another engineering which has demonstrated successful for

issue like meteorological computing, DNS computing, board strategies for airplane wing load computation and numerous different issues of this class

OBJECTIVES OF THE STUDY

1. To study on Distinctive Features of Parallel Computing
2. To study on Parallel Computing a natural tool for handling large problems of Mathematical Physics

REVIEW OF LITERATURE

Sinha U N et al (2010) The principal machine worked under the Flosolver project was Flosolver Mkl. It was likewise India's first parallel PC. It depended on the Intel 8086 microchip with coprocessor Intel 8087 working at a clock pace of 8 MHz. The PC had two hubs each having four such processors interlinked with the assistance of MultibusI and every one of the communications between the processors were done through a 512 KB shared memory. The between hub communication was finished utilizing the parallel port.

A few parallelized codes in Computational Fluid Dynamics (CFD) including Transonic Small Perturbations condition, the Navier—Stokes condition, 2-D rainstorm model were operational on this machine This was likewise the primary parallel PC on the planet with off the rack transport and the underlying achievement of utilizing off the rack transport for communication was an unequivocal factor for the further forms of Flosolver arrangement of logical parallel computers. As improvement of Flosolver Mkl was driven by application, it is critical to have a brief look at these applications to put this advancement of Flosolver arrangement of parallel computers and further plan in context.

Barry Smith F. et. al. (2013) Despite the fact that the subtleties of mathematical arrangement of TSP isn't needed in the current setting, the general perspective on the issue, its answer strategies and the agreeability of the parallel handling assets should be laid out so an answer for the mechanical issue utilizing parallel computing methods becomes all-good and endeavors at innovative improvements might be found in context. It might likewise be commented that a common issue might be addressed utilizing numerous strategies, yet to settle utilizing parallel machines just those techniques should be viewed as which are amiable for parallel computing. For the majority of the actual issues area deterioration methods have become a characteristic decision where communication is required generally at the limits so the proportion of the volume of calculation to that of communication is essentially

higher, which is an essential prerequisite for the viability of parallel computing.

FloSwitch dependent on i486 (Flosolver group 1999), Pentium (Flosolver group 2002) and so on were created in various variants. In any case, each time a significant adjustment of the load up was required at whatever point change in processor was thought about. Additionally availability couldn't be expanded as the limit of the copper interconnects in creating clamor was should have been overseen. Albeit the troubles of the copper interconnects were overwhelmed by the utilization of optical interconnects, the calculations at the switch level were sequential that thusly was a wellspring of limits and bottleneck. To defeat the bottleneck, another procedure of utilizing the enormous door cluster assets on the FloSwitch was taken up. This expertise of using the computational capacity of the entryway assets could accomplish parallelism in the calculations at the switch level. The abuse of the communication ability of the door clusters was in sitting tight for this new switch. The current theory has the beginning in improvement of the computational piece of FloSwitch.

Richard Varga S (2015) The estimation of impact coefficient is finished just when documents from every one of the processors are combined appropriately. Having gotten the impact coefficients, the subsequent direct arrangement of conditions is next tackled. Note that Gauss-Seidel strategy embraced here must be changed appropriately to exploit the parallel computing office. In contrast to the impact coefficients, the answer for peculiarity strength on any board is subject to the upsides of the multitude of different boards. This makes for the continuous communication between the processors just as between the hubs. Since the between hub communication is more slow when contrasted with bury processor communication, just a single hub was utilized for settling the above set of direct conditions.

Venkaresh K S (2010) The message preparing ability of FloSwitch rolled out a subjective improvement in parallel handling with distributive memory engineering where crossbar availability was not needed. What could be managed with shared memory design or with distributive memory engineering or with crossbar network, was conceivable utilizing FloSwitch. To clarify it in solid terms, a quantitative model adjusted from reference is introduced underneath which brings out plainly the benefits of FloSwitch in viable 31 an applications.

RESEARCH METHODOLOGY

FloSwitch and its Optical Interconnect

The principal unassuming endeavor to expand the versatility of FloSwitch was made in 2004. The Processing Element (PE) is associated with the FloSwitch through standard interconnect agreeing the Peripheral Component Interconnect (PCI) convention.

As the copper based PCI is intended for brief distance communications, it was unrealistic to interface more than 4-8 PEs with accessible mastery in designing of interconnections, and manufacture at NAL. Henceforth, the interest for seriously computing force must be met by scaling and in this way it was fundamental to have huge number of processors in groups of 4 or 8 PEs with second degree of interconnections. Consequently processors were assembled into bunches of really four PEs associated with a FloSwitch as demonstrated in the figure 2 and interfacing these groups arose as the principle task for acknowledging improved computing power.

The interconnection of these FloSwitches requested a reasonable interconnect that couldn't just convey over longer distances for tackling space issues, however it had in particular the prerequisite to coordinate with the transmission capacity similarity issue. In synopsis, the interconnection was to meet the accompanying necessities:

- The interconnects should satisfy the data transfer capacity prerequisites.
- The interconnects should be dependable over sensible distance so the commotion issue, bundling and space issue ought to be monitored; lastly,
- The interconnects should be viable for use with the FloSwitch

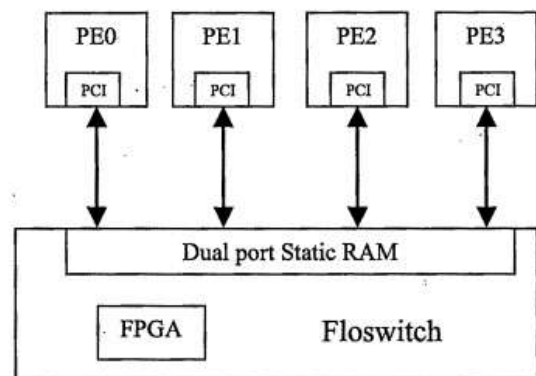


Fig 2. Inter connection of PEs in a typical cluster.

In the interceding years, regularly from the mid 2000 the technology of optical communication developed greatly (Robert Bradley 2007). Specifically, the off the-rack rationale clusters worked by producers like Xilinx, Altera, Lattice Semiconductors, Actel, Silicon Blue Technologies and so forth empowered the structure of Optical - Electrical - Optical (O - E - O) based optical switches. Here the information signal goes through transformation among optical and electrical spaces. The semiconductor handsets utilize laser based Light Emitting Diode (LED) that changes over the electrical signs into the optical comparable for transmission and a Photodiode is

utilized to change over the optical sign into its electrical identical at the recipient. The rationale clusters in the electrical space that contain the computational capacity are utilized for preparing and the optical area are utilized for communication.

The table 1 shows the data transmission examination of communication path in a run of the mill group of Flosolver arrangement of parallel PC. Here the PCI based information move from the PEs to the Floswitch at full burden activity for 64 pieces (8 bytes) information move at 66MHz gives the transfer speed of $66 \times 8 = 528$ Mbytes/sec. The Floswitch working at 78.125 MHz moves a 64 pieces information from SRAM with two banks at the information pace of $78.125 \times 8 = 625$ Mbytes/sec, which is more noteworthy than that of the PCI based interconnect of the PE. Thus, the interconnect ought to have a transmission capacity more prominent than that upheld by the Floswitch. The transmission capacity of the optical interconnect utilized in Flosolver Mk6 (Minutes of the second gathering 2008) which has the pinnacle working bit rate at 6.25 Gbits/sec, was at $6250/8 = 781.25$ Mbytes/sec that matches serenely with the necessities of the interconnects utilized in the groups of Flosolver arrangement of parallel computers and is additionally solid for significant distance communication.

Table 1

Bandwidth requirement	
PCI based PE	528 Mbytes/sec
Floswitch	625 Mbytes/sec

Technological Aspects of the Optical Link in Flosolver series of Parallel Computers

The mix of Floswitch alongside the optical switch turned into the remarkable component of communication instrument in the Flosolver Mk6 framework. The utilization of optical communication made it conceivable to accomplish a supported computational speed of !4 TFLOPS. The optical switch in Flosolver Mk6 was at first evolved utilizing a SERIALiser-DESerialiser (SERDES) chip that was utilized for sequential communication and the signs were sent utilizing an optical connection through various channels. This brought about setting up the association with interconnect numerous FloSwitch, so that huge number of PEs could be associated (Arvinda KM et al 2003).

Performance Index of Optical Interconnects

The presentation of optical communication in the Flosolver arrangement of parallel PC opened the opportunities for the plan of more proficient and minimal interconnects. The most recent rendition of

Flosolver arrangement of parallel PC the Flosolver Mk8 expected to have 1024 processors interconnected to one another necessary an enormous interconnection network with negligible overhead for information move. All things considered, the FPGA with more number of channels could be utilized to meet the interconnection necessities of enormous number of groups.

DATA ANALYSIS

Message Processing in the Floswitch

The Floswitch in Flosolver arrangement of parallel computers has been a result of another worldview of message communication and message preparing taking into account issues identifying with parallel computing of firmly coupled issues. In this worldview, communication switch measures data while imparting and this outcome in another design which has demonstrated extremely powerful for issue like meteorological computing, DNS computing, board methods for airplane wing load computation and numerous different issues of this class. The adequacy of this methodology can be effortlessly evaluated by really straight accelerate of Navier Stokes estimation which is something like an achievement in making a decision about viability of parallel computing (Venkatesh T N et al 2005). The basics and bits of knowledge of the adequacy of Floswitch are as yet not usually found in the writing thus even at the danger of repetition one might want to cause to notice the toy issue of adding an exhibit to clarify the design includes with the goal that the center substance of the fundamental thoughts can be placed into appropriate viewpoint.

Existing Message Processing Implementation

As seen in part three, the plan of Floswitch in Flosolver Mk8 has incorporated highlights of Floswitch of Flosolver Mk6 and Flooptilink switch of Flosolver Mk6 into a solitary communication switch with more number of Programmable Logic Blocks (PLBs) alongside the rapid information communication support. The microchip based Floswitch, however passages a long ways ahead in examination with group based engineering, the reality stays that it executes the directions sequentially for message preparing which indeed restricts the exhibition improvement. FloSwitch.Ph2 .Pentium.E2X (Minutes of the second gathering 2008), an Intel Pentium processor based form of Floswitch bears declaration to this perception. The computational ability of the door exhibit rationale that was instrumental to play out the arithmetical and legitimate activities needed for information handling in simultaneousness with the information transmission or gathering may additionally be abused for altered parallel and pipelined message preparing. This kills the previously mentioned

bottleneck of sequential calculation utilizing chip for message handling.

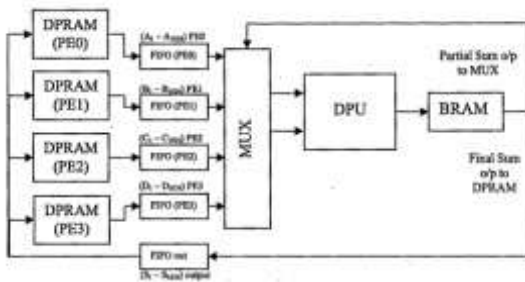


Figure 3 Block diagram of the Data Processing Engine in the Floswitch.

In real activity, information square of 1024 d words are utilized in Flosolver arrangement of logical parallel computers for application. Along these lines, we consider the 1024 dwords information in the first clarification. Leave information at each contribution of the PEs alone $A_i - A_{1024} \gg B_i - B_{1024} C_i - C_{1024} D_i D_{1024}$ for PE0, PE1, PE2 and PE3 individually and the amount of information from every one of the PEs be $S_i - S_{1024}$ as demonstrated in the figure 3. Here $A_i + B_i$ structures the halfway outcome and this outcome is added with C_i to frame an incomplete outcome again and afterward it is added with D_i to give the end-product S_i . Every one of the fractional outcome and the outcome are gotten in resulting clocks. In this way, the amount of one bunch of information from every one of the PEs S_i require 3 timekeepers when the information is free in the particular FIFOs

CONCLUSION

Handling of one bundle information (1024 dwords) includes the accompanying advances: 1. One read check is needed to peruse information from every one of the four recollections of the separate PEs to the info cradle. Since every one of the PEs have diverse memory impedes, these read are acted in parallel. Along these lines, 1024 dwords read will take 1024 clocks. The calculation of input information from each of the four PEs in the most ideal case is 3 tickers. Here, 1024 dwords from every PE requires $3 \times 1024 = 3072$ tickers. 3. Finally, one compose clock is needed to compose every resultant dword from the yield BRAM to the individual recollections of the multitude of separate PEs in broadcast. Consequently, 1024 dwords compose requires 1024 tickers. In this way, the total activity for a parcel of information comprising of 1024 dwords requires $1024 + 3072 + 1024 = 5120$ timekeepers. The new plan of the Floswitch has been developed that is better than every one of the variants and has the presentation practically identical with that of the InfiniBand. It very well might be pointed from Chapter 4 that Floswitch uses PCI interface for information communication with the PE's that has a greatest information pace of 528Mbps. The use of PCIe interface will conquer this bottleneck and improve the information rate upto 3.125 Gbps or more

per channel even with an optical interconnect that would be a critical improvement.

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