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Study of Different Analog Circuits in Udsm (Ultra Deep-Submicron Cmos)

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ABSTRACT:-

Modern and future ultra-deep-submicron (UDSM) technologies introduce several new problems in analog design. Nonlinear output conductance in combination with reduced voltage gain pose limits in linearity of (feedback) circuits. Gate-leakage mismatch exceeds conventional matching tolerances. Increasing area does not improve matching anymore, except if higher power consumption is accepted or if active cancellation techniques are used. Another issue is the drop in supply voltages. Operating critical parts at higher supply voltages by exploiting combinations of thin- and thick-oxide transistors can solve this problem. Composite transistors are presented to solve this problem in a practical way. Practical rules of thumb based on measurements are derived for the above phenomena.

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I. INTRODUCTION

The evolution in CMOS technology is motivated by decreasing price-per-performance for digital circuitry; its pace is determined by Moore's Law. To ensure sufficient lifetime for digital circuitry and to keep power consumption at an acceptable level, the dimension-shrink is accompanied by lowering of nominal supply voltages. While this evolution in CMOS technology is by definition very beneficial for digital, this is not so for analog circuits [1]-[3].

Contemporary ICs are mixed-signal systems consisting of a large digital core including amongst others a CPU or DSP and memory, often surrounded by several analog interface blocks such as I/O, D/A, and A/D converters, RF front ends, and more. From an integration point of view all these functions would ideally be integrated on a single die. In this case the analog electronics must be realized on the same die as the digital core and consequently must cope with the CMOS evolution dictated by the digital circuit. This paper discusses a number of issues for analog designs in modern and future ultra deep submicron (UDSM) CMOS processes and possible ways to maintain performance [3].

CMOS evolution has come to a point where for analog circuits new phenomena need to be taken into account. A major issue is the decreasing supply voltage. Although the supply voltage has dropped from 5 V in the early nineties down to 1.2 V today, most analog circuits can still be designed. However, a further drop in supply voltages is expected to cause serious roadblocks for analog circuits, because the signal headroom becomes too small to design circuits with sufficient signal integrity at reasonable power consumption levels. Although the analog transistor properties do not really get worse when comparing them at identical bias conditions, lower supply voltages require biasing at lower operating voltages which results in worse transistor properties, and hence yield circuits with lower performance.

A second issue is gate leakage. Gate leakage will increase drastically when migrating to newer technologies. When the gate oxide thickness is reduced with the equivalent of one atomic layer, the gate current increases by approximately one order of magnitude. Despite technological

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remedies, gate leakage will become part of analog design-especially for long transistors; e.g., in 65 nm technology the current gain of a MOSFET will be as small as unity for a channel length of 30 fim. In this paper, we introduce a bias insensitive frequency for quick estimation of the effect of gate leakage. Another issue is gate leakage current mismatch. For large area (long *L)* transistors mismatch will be dominated by gate leakage mismatch. This effect puts a new upper limit on achievable matching performance. This problem can be coped with by accepting increased power consumption or by using active cancellation techniques.

This paper is organized as follows. Section II reviews the implications of going to lower supply voltages. Section III discusses the trend in a number of bare transistor properties, also illustrating that lower supply voltages degrade circuit performance. In Section IV $/_{gate}$ is introduced while its use and applications are discussed in Section V. Section VI discusses a solution for the reduced nominal supply voltage aspects of newer CMOS generations: operating analog circuits at relatively high voltages, using thick oxide transistors and composite high-voltage transistors.

II. FUNDAMENTAL IMPLICATIONS OF LOWER SUPPLY VOLTAGES

From a circuit point of view, plain physics dictates that the power consumption of analog circuits is proportional to the level of signal integrity (e.g., the signal-to-noise ratio, SNR, or the signal-to-noise and distortion ratio, SINAD) and to the signal frequency [4]-[6]. In other words: for analog circuits more performance comes at the cost of higher power consumption. There is a factor between the actual and the fundamental minimum power consumption that takes into account implementation overhead, margins in operating conditions and device spread. A common observation in all power-performance relations is that power consumption rises with decreasing supply voltages. Appendix A presents a short review of a number of

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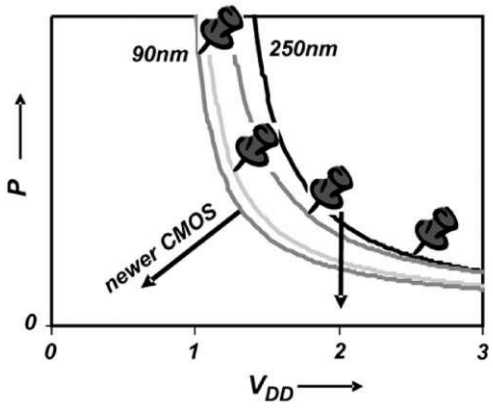

Fig. 1. Minimum power consumption for an (arbitrary) analog circuit (see Appendix A) with fixed topology and performance as a function of the supply voltage, for four technologies. Pushpins correspond to the power consumption in a technology at the nominal supply voltage for each CMOS process.

power-performance relations and discusses exceptions to the "rule."

For a given power budget the performance drops when migrating to newer technologies, simply because of their lower supply voltages. This is probably the single most important effect that (fundamentally and practically) complicates analog designs at low supply voltages. For Fig. 1, a simple unity gain voltage buffer with fixed topology, fixed performance and fixed technology was optimized for minimum power consumption; see also Appendix A. In the optimization process, signal swing, all bias conditions of transistors and device dimensions were optimized [6]. It follows that the minimum power consumption increases with decreasing supply voltages. However, *at constant supply voltage,* porting the circuit to a newer technology *lowers* the required power consumption.

III. A SOLUTION: LIVING OUTSIDE RAILS

The two major problems associated with analog circuit design in UDSM technologies are the low supply voltage and the gate-leakage related effects. One strategy to deal with the low-supply drawback is to operate critical parts of analog circuits at a supply voltage significantly higher than the nominal supply voltage for the CMOS process used. This typically reduces the power consumption significantly at a given level of performance [19]—[21], but requires a focus on

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lifetime issues such as oxide breakdown [22], hot carriers [23], [24], NBTI [25] and junction breakdown [26]. Generally junction breakdown is not a major issue while hot carrier degradation does not play a significant role at supply voltages lower than 1 V. The other two effects need to be limited by a suitable limitation of terminal-pair voltages. Techniques known from high-voltage I/O circuits can be readily used for this. A brief review is presented at the end of this section.

Analog Circuits at High Supply Voltages: The effect of operation of analog circuits in UDSM CMOS at a high supply voltage, up to a few times as high as the nominal supply voltage VbD,nom for the process, is illustrated in Fig. 11. Both curves in Fig. 11(a) and (b) show the minimum power consumption as a function of the supply voltage, for a circuit in a CMOS technology at constant performance, with optimized bias settings and device dimensions for each technology and supply voltage [6]. In these figures, the upper curves (tech1) correspond to an older technology while the lower curve (tech2) is a newer technology. For analog, the migration to a newer CMOS technology with its associated lower nominal supply voltage results in increased power consumption at fixed performance, indicated by the a) arrow in Fig. 11(a). Note that the jump to another curve corresponds to going to another technology with the same circuit topology. However, implementing the circuit in such a way that it runs at a high supply voltage can significantly decrease power consumption; this is indicated by arrow b) in Fig. 11(b). For reliability reasons typically circuit overhead is required, resulting in the upward part of the b) arrow.

An obvious advantage of migration to more advanced CMOS technologies is that it enables selective application of low-voltage transistors with their specific advantages and disadvantages. Especially interesting is the digital computational power that can solve many deterministic analog inaccuracies (e.g., mismatch and distortion).

Running Analog Circuits at High Supply Voltages: For circuits operating at high supply voltages, a number of robust high- voltage-tolerant transistors can be used to replace the standard transistors that can only reliably operate up to nominal supply voltages.

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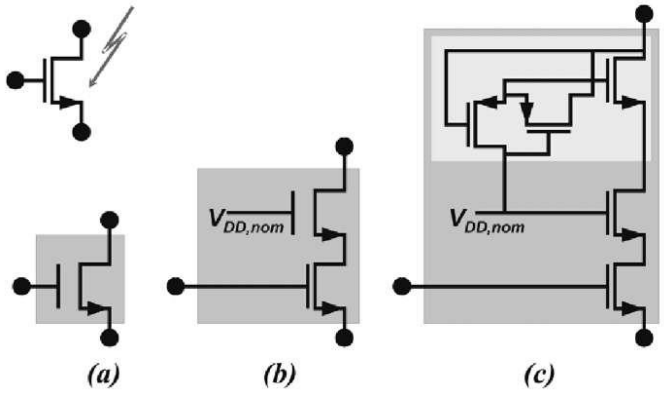

Fig. 12. Ways to implement high-voltage tolerant transistors in standard CMOS: (a) thick-oxide transistor; (b) (thick-oxide) cascode; (c) retractable cascode composite transistor.

Fig. 12 presents three examples known from high- voltage (HV) I/O circuits. A number of circuits and blocks with analog behavior implementing the retractable cascode HV transistors shown in Fig. 12(c) were discussed in [3] and [27]. These HV transistors enable direct reuse of most older circuit architectures, running at supply voltages corresponding to the original design: high supply voltages when related to the nominal supply voltage of the CMOS process used. Extended-drain transistors that can be realized in standard CMOS could also be used; such structures are described in [28].

The easiest way is to use the (commonly available) thick- oxide transistor [Fig. 12(a)] that is comparable to a two-generations-old standard transistor. However, in order to benefit from technology scaling compound structures using thin-oxide transistors, as in Fig. 12(b) or (c),[1] typically outperform the thick-oxide transistor in Fig. 12(a) in the fields of matching, $1/f$ noise and output impedance. These compound structures have some disadvantages: they are asymmetric, do not solve gate-leakage issues, and require suitable cascode voltages at power-up.

Careful selection of the analog sections to run at high supply voltages, and careful selection of the best type of transistor (thin oxide, thick oxide, or compound) will to a great extent circumvent one of the main roadblocks in UDSM CMOS technolgies: the low nominal supply voltage. Note that thick-oxide transistors also solve gate-leakage issues as their gate leakage is usually negligible.

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IV. CONCLUSION

Modern and future UDSM CMOS introduce several new problems for analog circuit design. From a fundamental point of view, lowering the analog supply voltage leads to an increase in power dissipation at constant performance. This increase in power dissipation becomes drastic as the supply voltage approaches the threshold voltage plus a few hundred millivolts, as illustrated in Fig. 1.

When migrating to modern technologies the quasi-dc analog transistor properties hardly change, as long as constant transistor lengths and terminal voltages are used. However, if the supply voltage is reduced according to the technology roadmap, the analog performance is lowered because of the lower bias voltages. Nonlinear output conductance in combination with reduced voltage gain pose limits with respect to linearity of (feedback) circuits.

Gate leakage becomes a serious problem in upcoming technologies, especially if long transistors are used. A parameter f_{gate} is introduced that enables quick estimations of gate-leakage related effects. Besides gate leakage itself, mismatch in gate leakage introduces new limitations. Mismatch cannot be tackled anymore by simply spending more area for transistors: when the transistor length L is increased an upper limit to matching is encountered. Here, increasing area does not automatically improve overall matching anymore, except if higher power consumption is accepted or active cancellation techniques are applied.

Operating critical parts at higher supply voltages, by exploiting combinations of thin- and thick-oxide transistors can solve the low voltage as well as the gate leakage problems. Composite transistors are presented in Fig. 12 to solve this problem in a practical way. In summary: unlike digital designs, analog circuits benefit from technology scaling if the supply voltages are *not* scaled down.

APPENDIX A

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In this Appendix, known performance-power relations for active circuits are briefly reviewed and their impact is discussed.

A. ***Performance in SNR: Total Integrated Noise***

A number of papers on the relation between analog performance and power consumption specify the performance in only its signal-to-noise-ratio (SNR) and the signal bandwidth [4], [5]. Typically, only the total integrated thermal noise is taken into account. In these papers, a system as depicted in Fig. 13(a) is used: an unspecified analog circuit represented by a resistance or conductance.

Including only thermal noise integrated over the total noise bandwidth of the circuit, the integrated noise voltage and the required (class-A) bias current are

$$\bar{v}_n^2 = \frac{kT}{C} \quad \text{and} \quad I_{\text{bias}} = 2\pi f_{\text{sig}} C \hat{V}.$$

These equations lead to a minimum power consumption of an analog circuit given by

$$P = \frac{8\pi kT \cdot \text{SNR} \cdot f_{\text{sig}}}{\eta_{\text{vol}} \cdot \eta_{\text{cur}}}$$

where η_{vol} is the ratio between the peak-peak signal swing and the supply voltage [15], η_{cur} is the efficiency of using supply current [15], kT are Boltzmann's constant and the temperature, respectively, SNR is the circuit's signal-to-noise ratio as a power ratio, f_{sig} is the signal frequency, V is the signal amplitude.

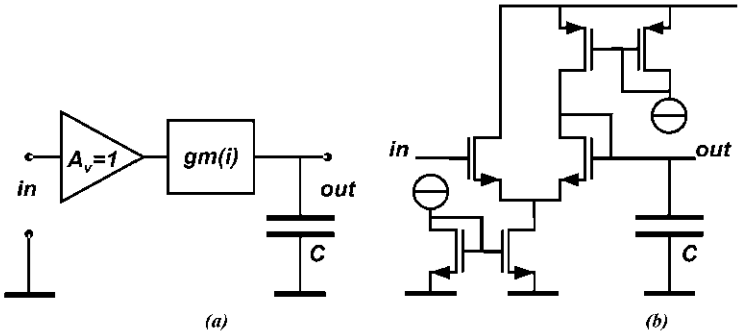

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Fig. 13. (a) Circuit representation assumed for the power-performance relations: a circuit with an output resistance and an output load, and (b) actual circuit topology used in [6].

Taking into account only thermal noise, the power consumption required for some SNR is technology independent if both the parameters ?7$_{vo}$i and 7/$_{cur}$ are invariant over technology. In general, f]$_{vo}$\ and r]$_{cur}$ increase with newer technologies because of voltage overhead (e.g., to accommodate gate-source overdrive voltage and saturation [15]) and due to the use of folded structures.

B. Performance in SNR: Bandwidth Limited Noise

For many circuits the total integrated thermal noise at the output is irrelevant: only the noise within some frequency band is of interest. In this case, neither the thermal noise nor the required bias current is related to the output capacitance: this capacitance is now purely parasitic. For this type of circuit, the integrated thermal noise voltage is[2]

$$\bar{v}_n^2 = \frac{4kT}{gm} BW$$

where *BW* is the relevant frequency band.

For ordinary active electronic components, the transconduc- tance g_m is a function of the bias current and of some voltage. For bipolar transistors and MOS transistors

$$g_m = \frac{qI_{\mathrm{BIAS}}}{kT} \quad \text{and} \quad g_m \cong \frac{2I_{\mathrm{BIAS}}}{v_{GT}}$$

where a lower bound to the effective gate-source overdrive voltage v_{GT} for MOS transistors is weak-inversion (bipolar-like) operation. These two expressions can be captured in one: $g_m = I_{\mathrm{BIAS}}/v_{\mathrm{OD}}$ where v_{OD} is something like equivalent effective overdrive voltage. The minimum power consumption to reach a certain SNR is then

$$P = \frac{16kT \cdot \mathrm{SNR} \cdot BW}{\eta_{\mathrm{vol}} \cdot \eta_{\mathrm{cur}}} \cdot \frac{v_{\mathrm{OD}}}{\widehat{V}}.$$

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It also follows that the power consumption is proportional to the targeted SNR. However, lowering the supply voltage (and signal swing) without decreasing the v_{OD} increases the required power consumption. Note that this situation always occurs with bipolar transistors and MOS transistors in moderate or weak inversion.

C. Performance in SINAD: Total Integrated Noise

In many analog circuits, both noise and distortion are relevant to the performance. For those circuits the signal-to-noise-and- distortion ratio (SINAD or SNDR) may be the right way to express the performance. Examples of circuits for which this type of performance is relevant include switched-capacitor circuits and track-and-hold circuits. The circuit corresponds to that in Fig. 13(b). In general, it is an unspecified analog circuit driving an explicit load capacitance as shown in Fig. 13(a). The actual analog circuit can be anything ranging from a nonlinear resistance to an analog amplifier with any amount of global or local feedback. In [6], it was shown that, taking the total integrated thermal noise into account, for weakly nonlinear analog circuits with a dominant load capacitor the absolute minimum power consumption is

$$P_{\min} = 2 \cdot \hat{V} \cdot gmi\left(2kT \cdot \pi \cdot f_{\text{sig}} \sqrt[n]{\frac{2\alpha_n}{\hat{V}}} \cdot \text{SINAD}^{\frac{2n+1}{2n}} \cdot \frac{(2n+1)^{\frac{2n+1}{2n}}}{n\hat{V}}\right)$$

where n is the ordinal number of the dominant harmonic, α_n links higher harmonics to the first harmonic[3] as $h_n = \alpha_n (h_1)^n$, and $gmi(g)$ is the inverse of the function between the conductance and bias current of a circuit.

In the derivation of this expression, distortion, and noise are traded against each other in such a way that a maximum performance-power consumption ratio is reached. Note that this general expression is much more complex than its SNR- based counterpart, presented in Section A. For ordinary weakly nonlinear analog circuits, substituting the $gmi(x)$ function and α_n results in a circuit-specific SINAD-P relation with many similarities to the SNR-P relation mentioned above; see [6]

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for two examples. The biggest difference between the SNR expression and the SINAD expression is that the latter contains a multiplicative term that increases with decreasing signal swing, and hence with the lower supply voltage that comes with newer CMOS generations. With the assumptions leading to the SNR limit (marginally preventing both clipping and slewing) straightforward mathematics shows that the complex SINAD-P expression collapses to the SNR-P one[4] in Section A:

$$\lim_{n\to\infty} P_{\min} = 8\pi kT f_{\text{sig}}\,\text{SINAD}|_{D\ ,0} \equiv 8\pi kT f_{\text{sig}}\,\text{SNR}.$$

D. *Performance in SINAD: Bandwidth Limited Noise*

For circuits dealing with a SINAD performance specification, either the total integrated noise or bandwidth limited noise may be relevant. In the case of bandwidth-limited noise, there is no need for an explicit load capacitance. As a direct consequence of the absence of any required bandwidth limitation, from a mathematical point of view harmonic distortion is zero. The relation between power consumption and bandwidth-limited SINAD therefore equals the relation for power and bandwidth-limited noise under B.

E. *Summary*

From a fundamental point of view it can be concluded that lowering the supply voltage increases the power-performance ratio, with exception of the simplest case described under A. Moreover, any voltage overhead ΔV worsens the power-performance ratio with decreasing supply voltage V_{DD}, typically introducing a multiplicative term $V_{DD}/V_{DD} - \Delta V$ in the power relation.

F. *Exceptions to the Rule*

Most analog circuits comply with the power-performance relations discussed here. Obvious exceptions to this rule are circuits that are overly robust in some aspect, for example most flash A/D converters that minimize mismatch issues by spending area, or that cannot satisfy some scaling issues, e.g., low-noise amplifiers.

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Flash A/D Converters: Practical findings indicate that the power consumption in flash A/D converters is not determined by thermal noise issues, see, e.g., [15]. Typically, low-resolution flash converters aim to reach a certain level of matching, by spending area, at some operating frequency. Under these conditions matching and speed requirements determine the power consumption, and consequently the power consumption of flash A/D converters decreases with newer CMOS generations because of better matching properties. However, when using active matching techniques [15], [29], [30], the need to spend area for matching is absent and the power-performance relation is determined by SNR issues again [15]. Note that it is a fundamental property of dc-type disturbances that no power is needed for their minimization. The apparent independence of SNR and power consumption in flash A/D converters is therefore due to the practical way mismatch is dealt with.

Low-Noise Amplifiers: Other circuits that do not comply with the discussed power-performance relations include RF low-noise amplifiers (LNAs). In the derivation of these relations, the signal swing is optimized for a given supply voltage. However, in LNA-type circuits the signal swing is fixed and lower supply voltages result in somewhat degraded bias circuitry and in a lower implementation overhead [15]. The overall result is that for circuits with a fixed very low signal swing, the power-performance ratio can improve with newer CMOS generations [31], [32].

APPENDIX B

Using a simplified relation for gate current based on the gate current model in MOS Model 11 [33], we can write the following relation for a MOSFET in saturation. In this relation, the effects of overlap regions are neglected:

$$i_{GS} = A \cdot v_{INV} \cdot v_{GS} \cdot \exp(B \cdot v_{GS})$$

where v_{INV} is the effective gate bias, given by

$$v_{INV} = m \cdot \varphi_T \cdot \ln\left(1 + \exp\left[\frac{v_{GS} - V_T}{m \cdot \varphi_T}\right]\right)$$

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and *A* and *D* are constants given by

$$A = \frac{I_{\mathrm{GINV}}}{2} \cdot \exp\left[-\frac{3}{2} \cdot \frac{B_{\mathrm{INV}}}{\chi_B}\right] \quad \text{and} \quad B = \frac{3}{8} \cdot \frac{B_{\mathrm{INV}}}{\chi_B^2}.$$

In the above, m determines the subthreshold slope (m = 1.3), χ_B is the oxide potential barrier($\chi_B = 3.1$ V for electrons, $\chi_B = 4.5$ Vfor holes), and /qinv and I?inv are physical parameters dependent on oxide thickness $t._{OX7}$ channel length *L* and channel width W. For electrons, we can write

$$I_{\mathrm{GINV}} = 1.6 \cdot 10^{-4} \cdot \frac{WL}{t_{\mathrm{ox}}^2} \quad t_{\mathrm{ox}} \text{ in [m]}$$
$$B_{\mathrm{INV}} = 2.9 \cdot 10^{10} \cdot t_{\mathrm{ox}} \quad t_{\mathrm{ox}} \text{ in [m]}.$$

As a simple approximation, we get the following expressions for the factors *A* and *B*, now with the oxide thickness in [nm] and assuming NMOS transistors. Note that gate current is proportional to the total gate area.

$$A = WL \cdot \frac{1.6 \cdot 10^{14}}{t_{\mathrm{ox}}^2} \cdot \exp(-14 \cdot t_{\mathrm{ox}}) \quad t_{\mathrm{ox}} \text{ in [nm]}$$
$$B = 4.5 \cdot t_{\mathrm{ox}}.$$

For the input capacitance C_{GG},we find (also neglecting the overlap regions) the following relation, where C_{OX} is the total oxide capacitance. Note that this term is also proportional to the gate area.

$$C_{GG} = \frac{2}{3} \cdot C_{\mathrm{OX}} \cdot \frac{\partial v_{\mathrm{INV}}}{\partial v_{\mathrm{GS}}} = \frac{2}{3} \cdot \frac{WL \cdot \varepsilon_{\mathrm{ox}}}{t_{\mathrm{ox}}} \cdot \frac{\partial v_{\mathrm{INV}}}{\partial v_{\mathrm{GS}}}$$

With $$\frac{\partial v_{\mathrm{INV}}}{\partial v_{\mathrm{GS}}} = \left(1 + \exp\left[-\frac{v_{\mathrm{GS}} - V_T}{m \cdot \varphi_T}\right]\right)^{-1}.$$

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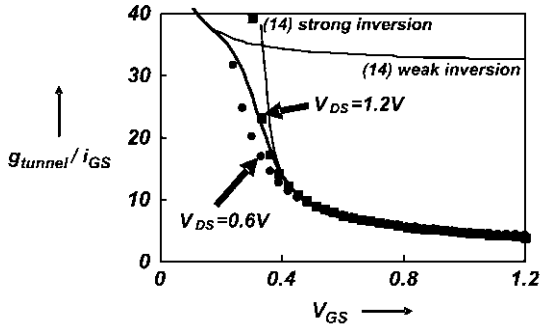

Fig. 14. Ratio g_{tunnel}/i_{GS} as a function of gate bias v_{GS}. Markers are measurement results and curves are predicted results using (13) and both expressions of (14).

The frequency where the imaginary part and the real part of the input impedance are equal is

$$f_{\text{gate}} = \frac{1}{2 \cdot \pi \cdot C_{GG}} \cdot \frac{\partial i_{\text{GS}}}{\partial v_{\text{GS}}}$$

with

$$\frac{\partial i_{\text{GS}}}{\partial v_{\text{GS}}} = A \cdot \exp(B \cdot v_{\text{GS}}) \cdot \left[v_{\text{INV}} \cdot (1 + B \cdot v_{\text{GS}}) + v_{\text{GS}} \cdot \frac{\partial v_{\text{INV}}}{\partial v_{\text{GS}}} \right].$$

it follows that in strong inversion and saturation, where $v_{\text{INV}} \approx v_{\text{GS}} - V_T$ and $\partial v_{\text{INV}}/\partial v_{\text{GS}} = 1$ and $C_{GG} = (2/3)C_{\text{OX}}$, f_{gate} for NMOS transistors can be approximated by

$$f_{\text{gate}} \cong \frac{\vartheta_{fgate} \cdot v_{\text{GS}}^2}{\exp(v_{fgate} \cdot t_{\text{ox}})} \exp(\zeta_{fgate} \cdot t_{\text{ox}} v_{\text{GS}}) \quad t_{\text{ox}} \text{ in [nm]}$$
$$\vartheta_{fgate} \approx 1.5 \cdot 10^{16} \text{ Hz/V}^2$$
$$v_{fgate} \approx 13.6/\text{nm}$$
$$\zeta_{fgate} \approx 1/\text{nm} \cdot \text{V}.$$

Similar relations can be derived for the moderate and weak inversion regions, and the linear region. For PMOS transistors f_{gate} is roughly a factor 3 lower due to the higher oxide potential barrier χ_B.

APPENDIX C

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The relation between gate conductance and gate current can be used in a number of expressions that link some gate-leakage related property to the size-independent f_{gate}. In this paper the properties discussed are the dc-current gain and the self-discharge droop-rate of MOS-capacitances. Using Appendix B, the tunnel conductance $g_{\text{tunnel}} = \partial i_{\text{GS}}/\partial V_{\text{GS}}$ can be readily calculated. The normalized gate conductance is then

$$\frac{g_{\text{tunnel}}}{i_{\text{GS}}} = \frac{\partial v_{\text{INV}}/\partial v_{\text{GS}}}{v_{\text{INV}}} + \frac{1}{v_{\text{GS}}} + \alpha_{gtun} \cdot t_{\text{ox}}$$
$$t_{\text{ox}} \text{ in [nm]}, \quad \alpha_{gtun} \approx 1.13/\text{nm}. \quad (13)$$

In strong inversion and weak inversion, respectively, this relation can be approximated by the following ones. Note that

the dimensions are correct because of implicit multiplication by appropriate scale factors.

$$\frac{g_{\text{tunnel}}}{i_{\text{GS}}} \approx \frac{1}{v_{\text{GS}} - V_T} + \frac{1}{v_{\text{GS}}} + \alpha_{gtun} \cdot t_{\text{ox}}$$
$$t_{\text{ox}} \text{ in [nm]}, \quad \alpha_{gtun} \approx 1.13/\text{nm}$$
$$\frac{g_{\text{tunnel}}}{i_{\text{GS}}} \approx \frac{1}{m \cdot \varphi_T} + \frac{1}{v_{\text{GS}}} + \alpha_{gtun} \cdot t_{\text{ox}}$$
$$t_{\text{ox}} \text{ in [nm]}, \quad \alpha_{gtun} \approx 1.13/\text{nm}. \quad (14)$$

As an example, Fig. 14 shows measured data for a 10 ^m*10 ^m transistor in a 120-nm technology, with the more exact expression and the two approximations for the weak inversion and strong inversion region. Clearly the simple relations comply very well to measurements.

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