Study of Analog-To-Digital Converters in CMOS Technologies

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Introduction

In wireless systems, the desired channel must be selected in the presence of strong adjacent-channel interferers. This requires wideband analog-to-digital converters (ADC) that can digitize both the desired and adjacent-channel interferers, resulting in high-dynamic range (DR) requirements. Meanwhile, the advances in the CMOS process, combined with its economical advantages, is driving the integration of a complete wireless transceiver in baseline CMOS. The demand for greater throughput leads to digital modulation schemes of greater complexity combined with a greater signal band.

As a result, there is a strong trend to digitize wideband receivers. In this perspective, oversampled $\Sigma\Delta$ ADC modulators are suitable because the adjacent-channel inter- ferers fall into the same band as the shaped quantization noise (Figure 1). Then, the same digital filter filters out both the quantization noise and interferers. Furthermore, $\Sigma\Delta$ ADCs provide an effective way to implement high-resolution ADCs without stringent matching requirements or calibration.

A block diagram of a $\Sigma\Delta$ ADC is shown in Figure 2. Basically, the digital output of the modulator contains a representation of the input signal plus a quantization noise that is shaped so that the noise is small in the band of interest and large elsewhere[1].

To gain more insight into the choice of a suitable $\Sigma\Delta$ ADC topology for a specific application, the 2002-2004 period was surveyed and analyzed through publications. All selected publications related to $\Sigma\Delta$ ADCs are based on measurement results and not on simulation. The former discussion is based on single loop and cascaded loop analysis, multibits and single-bit usage as well as continuous-time and discrete-time 2A loop filter implementation.

$\Sigma\Delta$ ADC trend in 2002-2004

A common figure of merit (FOM) used to compare ADC design is calculated according to the formula:

$$FOM = \frac{Power}{2^{ENOB} \cdot 2 \cdot signalband} \qquad \text{Eq. 1}$$

where ENOB is the effective number of bits, calculated according to the peak signal-to- noise-and-distortion-ratio (SNDR):

$$ENOB = \frac{SNDR|_{dB} - 1{,}76}{6{,}02} \qquad \text{Eq. 2}$$

The FOM is expressed in picojoules per conversion (pJ/conv.)

The power number specified in the publications is questionable. Sometimes a paper includes reference source, onboard oscillator and biasing circuitry in addition to the $\Sigma\Delta$ ADC's core. This can be inaccurate, but because the $\Sigma\Delta$ ADC's power core is usually the dominant factor, the inaccuracy is believed to be small and will not significantly corrupt the FOM.

As illustrated in Figure 3, since 2003 there has been a trend to increase the bandwidth conversion. The main reason is the emergence of more signal-band, demanding wireless standards such as IEEE 802.11.

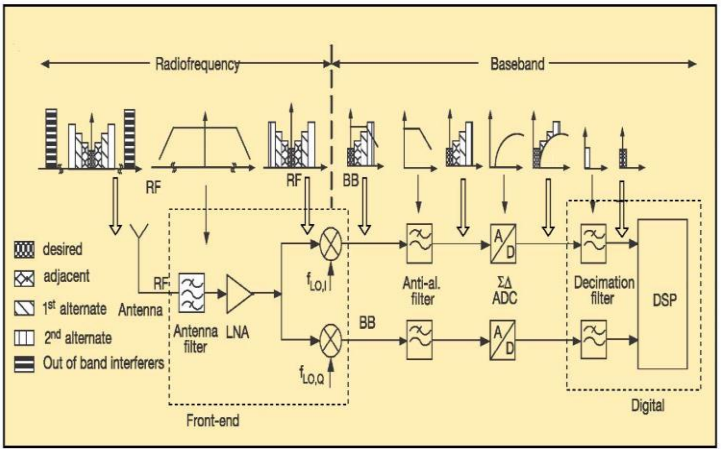

Figure 1. Direct conversion receiver with $\Sigma\Delta$ ADC.

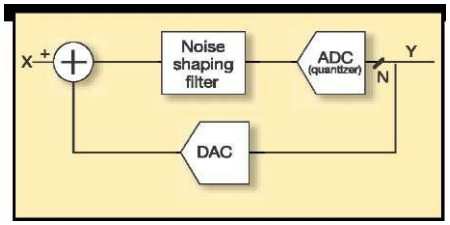

Figure 2. Sigma-delta $(\Sigma\Delta)$ ADC block diagram.

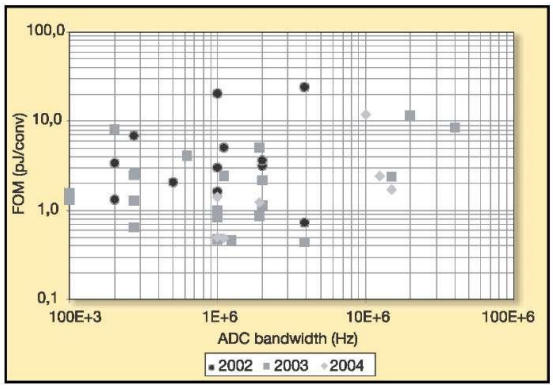

Figure 3. Surveying $\Sigma\Delta$ ADCs bandwidth limits.

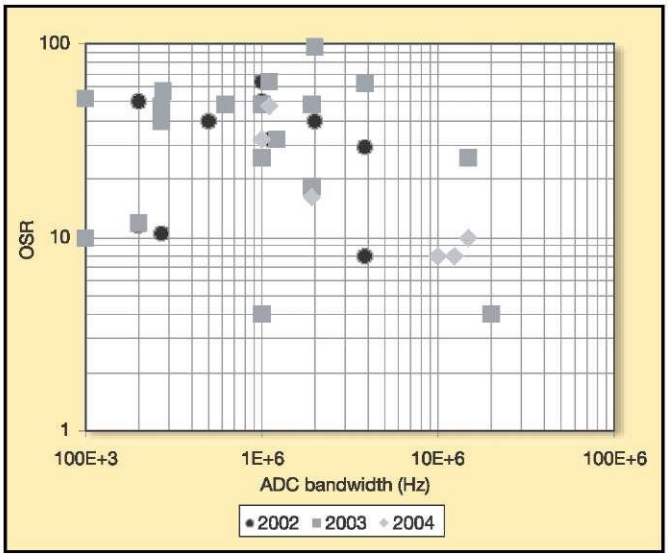

Figure 4. $\Sigma\Delta$ ADC OSR distribution as a function of bandwidth requirement from 2002 to 2004.

Despite the increase of conversion bandwidth, the FOM remains between 1 and 10 pJ/conv. Thus, according to Equation 1, the power consumption has been scaled down as well. The increase of conversion bandwidth and the decrease of power are two contradictory design targets. The simultaneous fulfillment of these two targets is a result of advances in process technology and circuit topologies. In addition, Figure 3 shows that when the signal band is

smaller than 10 MHz, then the $\Sigma\Delta$ modulator's FOM is limited by circuit noise—while it is mainly dominated by the technology performances when the signal band is larger than 10 MHz.

Typically, the sample frequency is limited to hundreds of megahertz for reasonable achievement and power consumption consideration in CMOS technologies. Consequently, as illustrated in Figure 4, an oversampling ratio (OSR) between 40 and 50 is acceptable for low (GSM) and moderate (Bluetooth and W-CDMA) bandwidth applications. However, for more demanding bandwidth applications such as WLAN, the OSR is typically lower than 10.

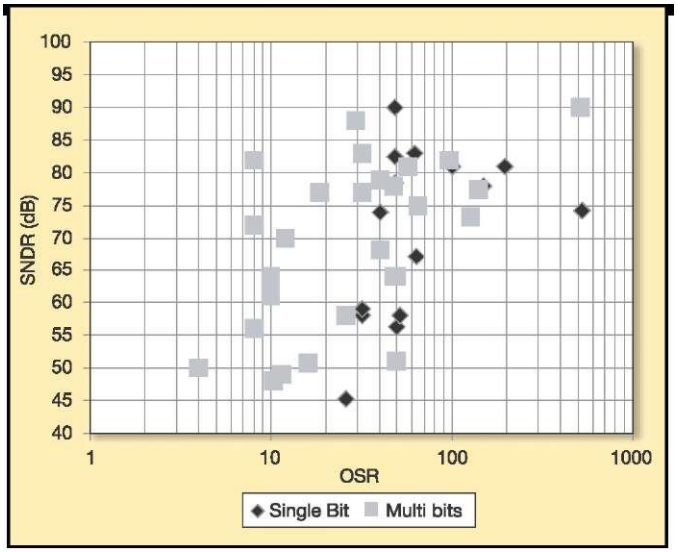

Figure 5. SNDR distribution of single bit and multibit $\Sigma\Delta$ ADC with respect to OSR.

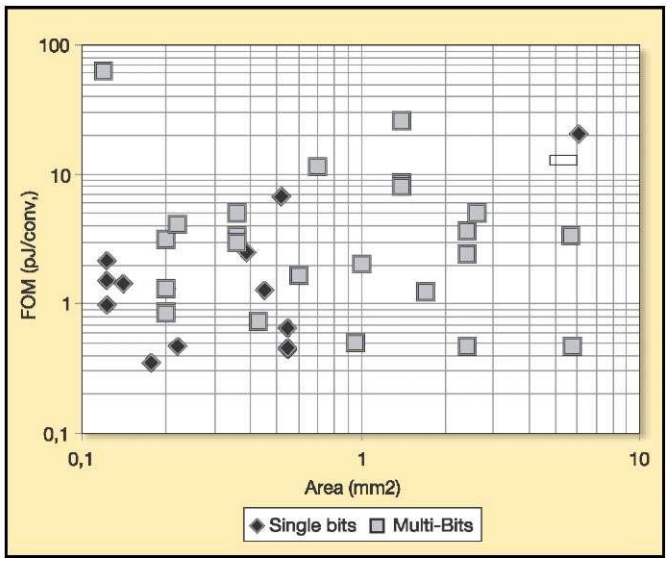

Figure 6. FOM distribution of single bit and multibit $\Sigma\Delta$ ADC with respect to area.

Multibits vs. single bit quantizer

The ADC resolution at a low OSR can be improved by using a higher-order loop filter, and/or by increasing the internal quantizer resolution. For single-bit, single-loop modulators, the integrator's gain must be reduced to preserve the loop stability. Therefore, simply increasing the loop filter order at a low OSR will result in a poor SNR improvement.

To achieve high resolution at a low OSR multibits internal quantization is widely used as illustrated in Figure 5. Since multibit quantizers have a more linear gain than single-bit quantizers, the stability of multibit, single-loop $\Sigma\Delta$ modulators is significantly improved. As a result, more aggressive noise transfer function can be designed, with the benefit of extra dynamic range for every additional bits *n* of [2]:

$$DR \propto 20 \log_{10}(2^n - 1) dB \qquad \text{Eq. 3}$$

Alternatively, increasing quantizer resolution enables us to use a lower noise-shaping filter for a given OSR. Unfortunately, it is necessary to double the number of comparators for each additional bit of quantizer resolution. Obviously, this costs silicon area as well as power dissipation and thus degrades the FOM for a given resolution as illustrated in Figure 6.

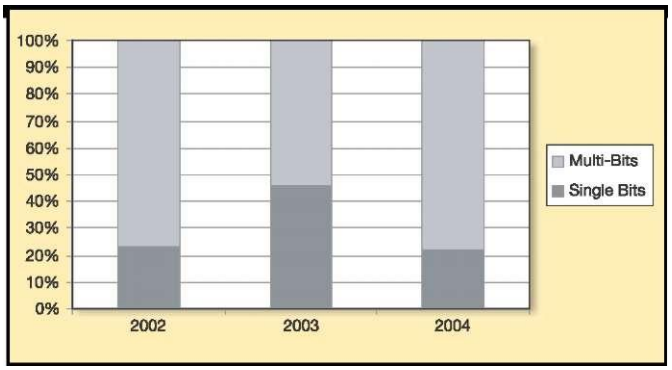

Figure. 7 Multibit and single-bit ΣΔADC distribution over 2002-2004 period

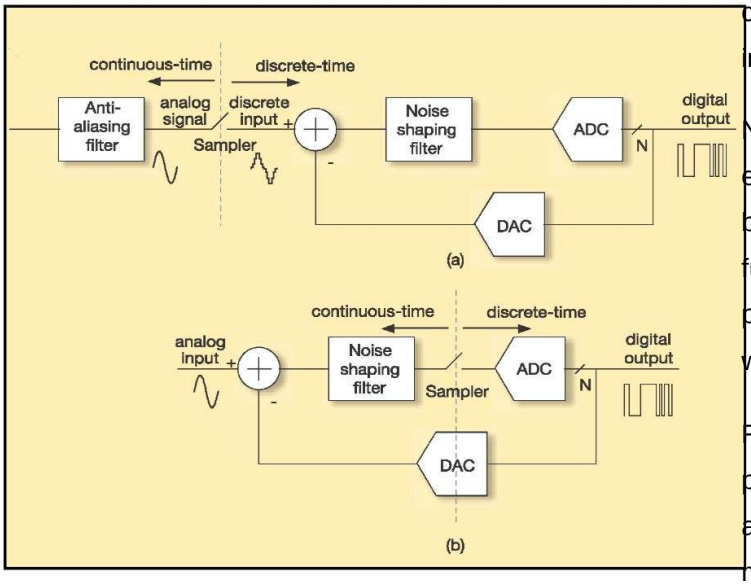

Figure 8. Block diagrams of a discrete-time (a) and continuous-time (b) ΣΔmodulator.

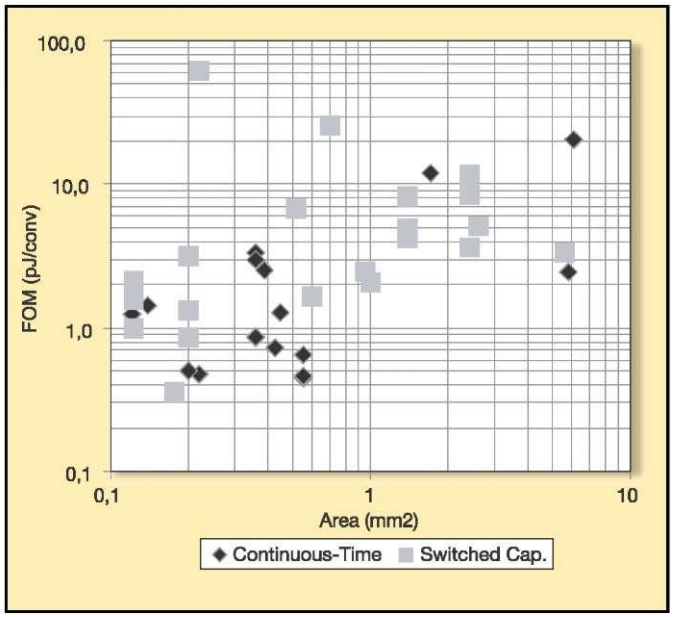

Figure 9. CT and DT ΣΔADC FOM distribution with respect to area.

In addition, multibit SD ADCs are sensitive to non-idealities such as mismatch in the feedback digital-to-analog converter (DAC), as these errors are added directly to the input signal and are thus not noise-shaped.

Nevertheless, deep-submicron technologies feature excellent matching characteristic as high as 11 bits or 12 bits of resolution. Hence, careful layout and design can fulfill linearity requirements of an internal-feedback DAC, provided that the ΣΔADC is lower than 12bit resolution, which is typically the case for W-CDMA.

For a ΣΔADC's resolution that exceeds the matching possibilities of CMOS or Bi-CMOS, this problem must be addressed. The solution consists of using dynamic element matching (DEM).

DEM converts the DAC element errors to high- frequency noise. Thereby, highly linear oversampling DACs can be built with only moderate matching requirements for the DAC element. DEM techniques have been developed

since 1998, starting with randomization of the DAC elements [4]. The methods are continuously improved with respect to implementation efficiency and order of shaping. Since the presentation of [5] in 1995 and the disclosure of the ADC design in [6] in 1997, these techniques have been well established in the sigma delta design community, allowing efficient and robust implementation of sigma-delta ADC's with resolution of more than 14 bits and bandwidth beyond 1MHz[7][8][9].

The digital complexity introduced by DEM— and more precisely the area and the power consumption penalty—is not believed significant since the mainstream CMOS process area is shrunk byL_{min}^2, i.e. 50%[10] every three years.

In addition, the power consumption in digital CMOS circuits scales with the square of the supply voltage[11], that roughly decreases by 20% at each technology node[10]. As a result, the superior DRperformances at a low OSR make multibit $\Sigma\Delta$modulators attractive for WLAN applications. Consequently, it is not surprising that in 2004 multibit design represented 78% of the published $\Sigma\Delta$ modulators (see Figure 7).

However, a detailed look at Figures 5 and 6 shows that single bit should be preferred to multibit $\Sigma\Delta$ADCs when the conversion bandwidth is lower than 5 MHz (GSM, Bluetooth, W-CDMA) because they achieved better FOM and are less silicon area-consuming.

Continuous-time vs. discrete-time

As illustrated in Figure 8, in an $\Sigma\Delta$modulator loop, it is possible to build up the noise-shaping filter as a discrete-time (DT) or a continuous-time (CT) circuit.

DT $\Sigma\Delta$ modulators are implemented using switched-capacitor (SC) circuit techniques. In SC circuits, amplifiers with high gain- bandwidth product (GBW) satisfy the settling requirements. Typically, the GBW is seven times higher than the sampling frequency. By nature, CT $\Sigma\Delta$modulators are not sensitive to settling behavior. As a result, CT $\Sigma\Delta$ modulators can potentially operate at higher clock frequency and/or with less power consumption. Note that in a CT $\Sigma\Delta$ modulator, the loop filter provides additional anti-aliasing filtering, which is beneficial when having to handle large interferers. In SC circuits, the in-band noise is bounded by the capacitor size. Consequently, and as illustrated in Figure 9, CT modulators have smaller FOM and are less silicon area-consuming than DT counterparts. Contrary to a CT modulator, in a DT modulator, large glitches appear on the op-amp virtual ground node of op-amps-RC integrators due to switching transient. Therefore, a CT modulator achieves better linearity performance. When the $\Sigma\Delta$modulator is integrated into a complete wireless transceiver in baseline CMOS, glitches generated in DT modulators can potentially couple to other critical blocks of the receiver, such as voltage-control oscillators (VCO), LNA and mixers, and can seriously degrade the receiver sensitivity.

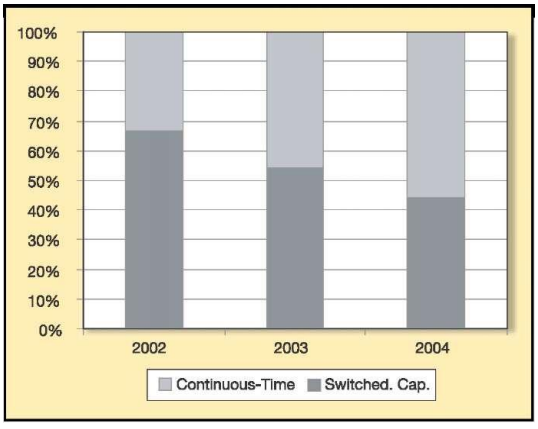

Figure 10. CT and DT$\Sigma\Delta$ ADC distribution over 2002-2004 period.

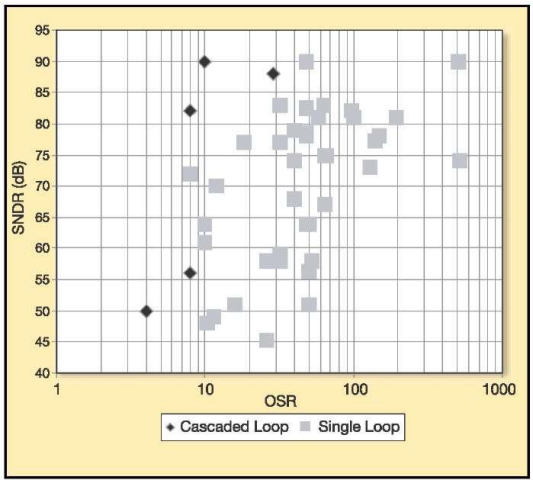

Figure 11. SNDR distribution of cascaded and single loops$\Sigma\Delta$ ADC with respect to OSR.

Today, CT modulators are preferred to DT modulators, whatever the application. This trend is illustrated in Figure 10, wherecontinuous-time implementation represents 55% of the published$\Sigma\Delta$modulators in 2004, whereas it was representing one-third in 2002 (see Figure 10).

However, it is well known that the clock jitter of the feedback DAC is critical in the SNR degradation of a CT single-bit feedback DAC. Some solutions should exist to circumvent the jitter effect. For example, going to an N-bits $\Sigma\Delta$ADC will reduce the quantization step by 2^N-1. Consequently, the DAC charge transfer fluctuation per clock period due to jitter will also decrease by 2^N-1. However, this solution is silicon area-consuming.

A more interesting solution consists of implementing an SC DAC while keeping a continuous-time loop filter. As demonstrated in [12], a return-to-zero clock scheme configuration associated with a settling time constant of the SC DAC eight times smaller than the clock period enables the decrease of jitter sensitivity by 4 dB. This latter solution is preferred for wireless applications that do not require more than 5 MHz conversion bandwidth because it optimally trades off the CT and DT advantages.

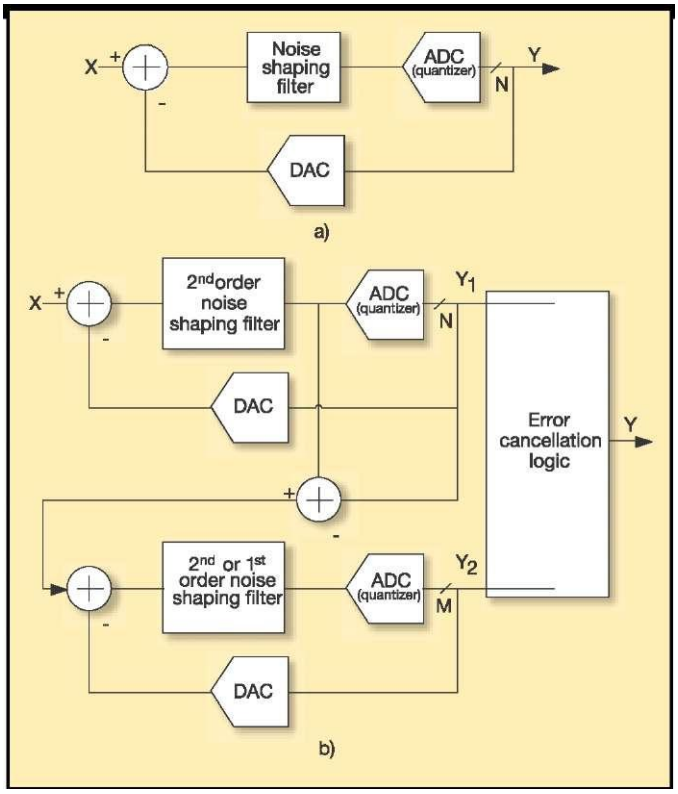

Figure 12. Single loop (a) and cascaded loop (b) $\Sigma\Delta$ modulator.

In a DT modulator, the time constant's variations of the noise- shaping filter achieve excellent matching since they rely on capacitor ratio. However, this is not the case in CT modulators where the time constant's variation is between 25% to 30% due to R and C spreads. This can seriously degrade the SNR performances. Nevertheless, some on-chip biasing techniques that consist of compensating the temperature dependence of hole or electron mobility in silicon enables the design of accurate time constraints

despite process and temperature variations[12]. Another solution widely used for op-amp RC integrator time constant tuning makes use of switchable capacitor arrays [13]. In this case, a calibrator is used to measure the fabricated RC product with a reference clock frequency. From this, a digital code word is generated, which is used to select elements in programmable arrays of capacitors that form the tuning elements of the filter integrators. Both solutions are robust and do not introduce too much circuit complexity.

Single loop vs. cascaded loop

Cascaded loops, also called MASH structure, are popular for high- dynamic range applications at low OSR (see Figure 11) because they facilitate higher-order $\Sigma\Delta$loops that do not suffer from stability problems.

However, cascaded modulators rely on good matching properties between analog and digital transfer functions. When the quantization noise of the first-stage quantizer is not fully cancelled in the digital error cancellation logic bloc (see Figure 12b) due to a non-ideal matching, leakage noise appears at the output of the modulator, rapidly decreasing the SNR performance. Typically, the leakage noise depends on analog circuit non-idealities, such as insufficient op-amp dc gain and gain factors spread over the temperature and the process variations. Moreover, cascaded loops are characterized by an inherent loss in dynamic range due to internal signal scaling.

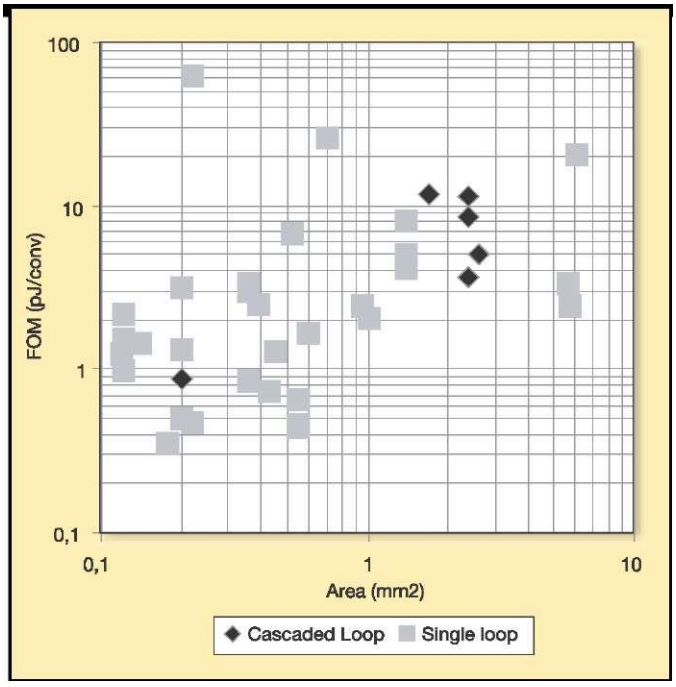

Figure 13. Cascaded and single loops $\Sigma\Delta$ ADC FOM distribution with respect to area.

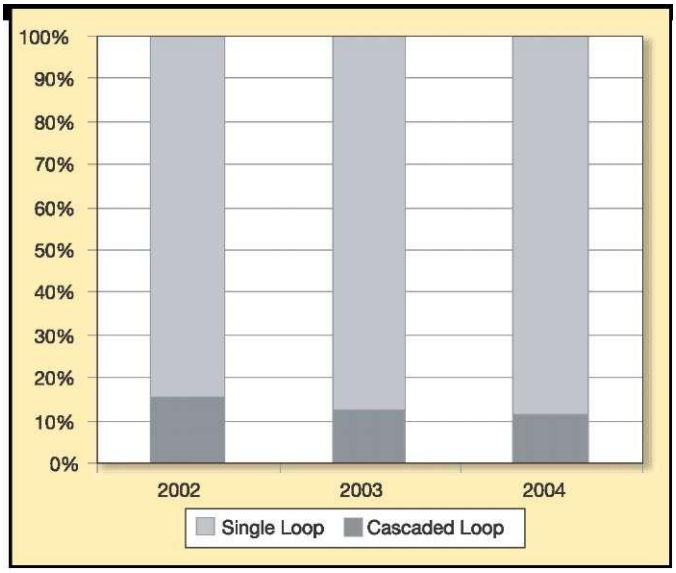

Figure 14. Single loop and cascaded loop $\Sigma\Delta$ADC distribution over 2002-2004 period.

These two factors impose constraints on the minimum size of analog components to the detriment of the parasitic capacitance and associated current consumption. Therefore, as illustrated in Figure 13, cascaded loops have larger FOM and are more silicon area-consuming than single-loop structures.

As illustrated in Figure 14, the cascaded loop fraction ofpublished $\Sigma\Delta$ modulators in the 2002-2004 period is decreasing by 2% every year and represents only 11% in 2004. One of the main reasons is the difficulty in designing op-amps with high dc gain in deep-submicron technologies.

Conclusion

The published $\Sigma\Delta$ADCs for wireless applications have been reviewed for the 2002-2004 period. Since 2003, there has been a strong trend to increase the bandwidth conversion while keeping reasonable clock frequency. This means that the OSR tends to decrease. As a result, multibit $\Sigma\Delta$ loops are preferred for bandwidth- demanding applications such as WLAN. However, single-bit $\Sigma\Delta$ modulators are recommended for wireless applications that require less than 5 MHz conversion bandwidth because they offer better trade-offs for power, area and circuit complexity. Moreover CT $\Sigma\Delta$ modulators are suited for a low-cost integration because they provide anti-aliasing filtering without silicon-area penalty and can potentially operate with less power consumption than DT implementation. At least, single loop topology is preferable in low-voltage, low-power designs because it is less sensitive to analog circuit non-idealities, such as insufficient op-amp dc gain that tends to decrease at each CMOS technology node.

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