Study on Process Flow in Mems

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Abstract – The first consideration is the choice of MEMS structural material. We use an insulator to provide high electrical and RF isolation between actuation and RF sections of the devices. To provide electrical contacts and electrodes for electrostatic actuation, conducting surfaces are formed on portions of this structural insulator. Thus our MEMS structures consist of sections that are composed simply of just an insulator and other sections where there is a tri-layer of conductor/insulator/conductor that is balanced to manage the stress.

Key Words; Conductor, Insulator, Electrodes, Electrostatic.

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INTRODUCTION

Many high-performance devices have been built using RF-MEMS including shunt and series switches (1, 2, 3), variable capacitors (4, 5), inductors (6, 7), and low-loss and variable transmission lines (8). However, these devices were developed in processes customized to build individual devices. RF-MEMS holds great promise for improving performance and increasing the integration of the RF front-end of wireless systems. The resulting narrow range of applications will not generate the volumes needed to justify the required foundry capital investment nor that needed to stabilize the process itself. While some standard processes exist (9, 10), they are unsuited for RF applications due to their resistive materials.

REVIEW OF LITERATURE

High performance passives are usually needed in groups within a RF sub-system, such as in tunable filters or in phase shifters. A process suitable for integration must be able to build all of these in one chip where each of the devices maintains its high performance and where the various devices can be interconnected with low loss to maintain the high-performance of the overall circuit. Another obstacle has been high-temperature processing that limited monolithic integration with active circuitry. This paper presents a flexible manufacturing process flow that addresses these shortcomings and details high performance devices created in the process.

MATERIAL AND METHOD

RF-MEMS require high quality metals and insulators for state-of-the-art well-controlled RF characteristics. All of our materials needed to have the following properties:

Low deposition temperature (300 C) to allow post-processing on CMOS

High etching selectivity

Low stress and stress gradients

Precise patterning techniques

Low cost deposition of thick (> 3 µm) layers

Available inter-layer adhesion layers

The sacrificial material has been chosen to provide uniform smooth layers, good step coverage, fast complete removal from thin gaps, formation of stacked patterned layers for vertical topography and additional functionality when intentionally protected from release etch.

There are three basic applications of metal in RFMEMS: buried conductors, exposed electrodes, and electrical contacts. Our choice of copper for the buried conductors was driven by:

Highest bulk conductivity (> $4 * 10^7$ S/m)

Corrosion resistance to processing steps

Available CMP process

Since electrodes and electrical contacts are both exposed, we have chosen to use the same metal for both. Our choice of Au-based metal was driven by:

Low contact resistance (< 0.5 ohms)

Low contact force (< 200 uN)

High melting temperature (> 800C)

Low self-adhesion

Low catalytic activity

The choice of insulators was constrained by:

Low loss tangent (< .003) and DC conductivity

Low dielectric constant (< 5)

High breakdown field

High mechanical yield strength

Insulators considered included alumina, high-resistivity silicon, silica, various polymers and GaAs. Alumina and silica both fulfill all of the necessary requirements. Silica was chosen due to immediate process availability within the candidate foundries.

Another consideration is the choice of substrate. The process enables device designs that are relatively substrate independent. Thus we can fabricate high performance passives, switches and other MEMS directly on top of functional electronic circuits, both passive and active, even on a resistive substrate. The complete range of compatible substrates is limited by thermal expansion, although these are not severe due to the low temperatures. All initial work has used low-resistivity (< 10 ohm-cm) silicon substrates.

PROCESS FLOW

The nominal process stack is shown in Figure 4.1. The overall flow is divided into three main sections: substrate connect, thick metal and thin metal. The substrate connect layer is used to make electrical connections to underlying circuitry and provide a planarized surface for further processing.

The thick metal section, used primarily for passives and interconnects, is composed of copper embedded in silica. This is built up in 7 µm thick layers composed of a nominal 3.5 µm sheet conductor and a 3.5 µm stud interconnect. Each layer is planarized using CMP. The nominal process uses two of these layers, yielding 14 µm of copper and/or silica, although more or fewer layers can be used to provide optimal complexity/cost tradeoffs.

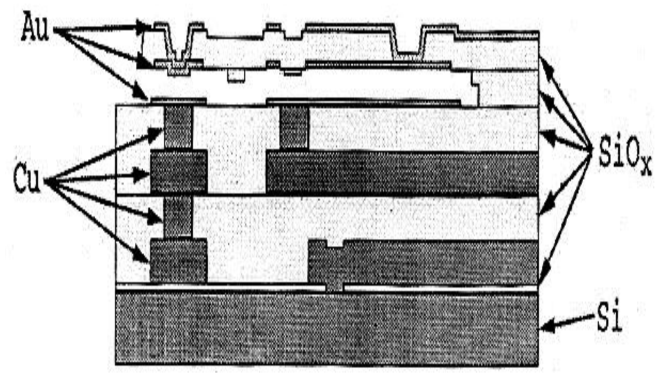

Figure 1: Multi-Function MEMS Process Stack

The thin metal section is composed of three layers of gold 0.5 µm thick that are used for electrodes and contacts, two layers of sacrificial copper that are 1.5 µm and 0.5 µm thick respectively and a 2 µm silica mechanical layer.

CONCLUSION

The process and the material properties determined from test structure extractions have been captured in CoventorWare™ for visualization and modeling of the 3D structure leading to straightforward electromechanical, damping and thermal simulations using CoventorWare™ and RF analyses using Ansoft's HFSS™.

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