

A Review about CMOS Technology Procedure to Development Connected With Ultra-Wideband Low Noise Amplifier

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Abstract – *This paper presents the configuration of ultra-wideband low noise amplifier (UWB LNA). The proposed UWB LNA whose transfer speed broadens from 2.5 Ghz to 16 Ghz is planned utilizing a symmetric 3d Rf mixed inductor. This UWB LNA has an addition of 11 ± 1.0 db and a Nf less than 3.3 db. Great data and yield impedance matching and exceptional confinement are accomplished over the working recurrence band. The proposed UWB LNA is determined from a 1.8 V supply. The UWB LNA is composed and recreated in standard TSMC 0.18 μm CMOS engineering procedure.*

INTRODUCTION

CMOS engineering is a standout amongst the most overarching advances utilized for the execution of radio recurrence coordinated circuits (RFICs) because of its decreased expense and its compatibility with silicon-built framework with respect to chip . The utilization of ultra-wideband (UWB) recurrence range (3.1-10.6 Ghz) for business requisitions was endorsed in February 2002 by the Federal Communications Commission. Low cost, lessened force utilization, and transmission of information at high rates are the focal points of UWB engineering. UWB engineering has numerous provisions, for example remote sensor and individual range systems, ground infiltrating radars, and restorative requisitions .

Low noise amplifier is acknowledged the spine of the UWB front-end Rf recipient. It is answerable for sign gathering and intensification over the UWB recurrence range. LNA has numerous wanted outline particulars, for example low and level noise figure, high and even power increase, exceptional data and yield wide impedance matching, high reverse seclusion, and lessened Dc power utilization.

These days a standout amongst the most suitable arrangements inferred for LNA usage is present reuse fell amplifier. This LNA arrangement can accomplish low Dc power utilization, high leveled addition, minimized Nf, and excellent reverse segregation while accomplishing wide info and yield impedance matching.

Radio recurrence mixed inductors assume a huge part in radio recurrence combined circuits (RFICs) implementation. Outline, improvement, and exhibition improvement of Rf combined inductors stand for a testing work. Realizing high mix level and take minimization of RFICs are discouraged as a result of the troubles confronting the Rf joined inductors originators which are identified with getting high caliber elements.

In this paper, the execution of LNAs utilizing 3d coordinated inductors will be examined. A symmetric 3d structure is proposed as another structure of reconciled inductors for RFICs.

This paper talks about the outline technique of current reuse fell UWB LNA and its transfer speed development. What's more, the livelihood of inferred symmetric 3d Rf mixed inductor will be showed. This paper is composed as follows. Segment 2 presents the inferred UWB LNA circuit.

CIRCUIT OUTLINE

As demonstrated in Figure, the proposed UWB LNA is a present reusecascadedcorebased on acommonsource topology with a shunt resistive input method brought about over the data stage.

This present reuse fell amplifier realized great wideband data impedance matching through the utilization of source degeneration data matching method. Figure shows the little sign identical circuit of this LNA data stage. The info port of

this UWB LNA is wanted to match source impedance R_s at reverberation recurrence ω_o . This matching circuit transfer speed is outlined through the quality components of source degeneration and pick up cresting inductors (L_s and L_g) where the data impedance is given by

$$Z_{in} = j\omega(L_s + L_g) + \frac{1}{j\omega C_{gs}} + \omega_T L_s$$

$$= j\omega(L_s + L_g) + \frac{1}{j\omega C_{gs}} + R_s,$$

where Z_{in} is the UWB LNA data impedance and ω_T is the present increase cut-off recurrence, where $\omega_T = g_m/c_{gs}$ and g_m and C_{gs} are the information stage transconductance and door source capacitance, individually. V_s stands for the R_f indicator source. R_s is the yield impedance of V_s .

In spite of the fact that the shunt resistive input circle prompts LNA noise exhibition corruption, it is considerably utilized as a part of as of late proposed LNAs because of its unrivaled wideband qualities. Shunt capacitive-resistive sentiment method is utilized to broaden the info matching transmission capacity and increment the LNA dependability.

Shunt-topped amplifiers are known to have wide pick up data transfer capacity and high low recurrence power addition. To have a high straightened increase of the proposed UWB LNA, shunt-cresting system is utilized. Likewise the door topping technique is utilized to improve the LNA increase at high frequencies. Also the shunt-and entryway topping systems, the shunt resistive input circle is utilized within addition smoothing. The LNA surmised increase is given by

$$A \cong \frac{V_{out}}{V_s}$$

$$\cong \frac{g_{m1} g_{m2} [R_f // (R_{d2} + S L_{d2})] [S L_{d1}]}{2 \cdot S C_{gs1} [S (L_{s1} + L_{g1}) + 1/S C_{gs1}]}$$

Ultra-wideband provisions require great noise performance notwithstanding high and level pick up. Low noise plan procedures which are suitable for narrowband provisions can't be utilized for wideband provisions. Principle commitment of fell matched stages noise figure is because of first stage. The decrease of noise figure of info stage will expedite the decrease of the general noise figure of the proposed outline. Advancement and control of elements influencing the N_f will enhance this UWB LNA noise exhibition. An equal circuit of the information stage for noise consider estimation is indicated in Figure.

An expected quality of the noise figure ($N_f = 10 \log_{10} f$) of this topology is given in where f is the noise variable of the UWB LNA. The noise component f could be given by

$$f = 1 + \frac{R_g + R_{lg} + R_{ss} + R_{ls}}{R_s} + \frac{\delta \alpha \omega^2 C_{gs1}^2 R_s}{5 g_{m1}}$$

$$+ \frac{R_{fB} ((L_{g1} + L_{s1}) C_{gs1})^2}{R_s (g_{m1} R_{fB} - 1)^2}$$

$$\cdot \left| s^2 + s \left(\frac{\omega_{o,rfbn}}{Q_{rfbn}} \right) + \omega_{o,rfbn}^2 \right|^2$$

$$+ \frac{\gamma g_{m1} (R_{fB} + R_s)^2 ((L_{g1} + L_{s1}) C_{gs1})^2}{\alpha R_s (g_{m1} R_{fB} - 1)^2}$$

$$\cdot \left| s^2 + s \left(\frac{\omega_{o,dn}}{Q_{dn}} \right) + \omega_{o,dn}^2 \right|^2,$$

$$f = 1 + \frac{R_g + R_{lg} + R_{ss} + R_{ls}}{R_s} + f_{gn} + f_{rfbn} + f_{dn},$$

where

$$\omega_{o,rfbn} = \sqrt{\frac{1 + g_{m1} R_s}{(L_{g1} + L_{s1}) C_{gs1}}},$$

$$Q_{rfbn} = \frac{1}{R_s + \omega_{T1} L_{s1}} \cdot \sqrt{\frac{(1 + g_{m1} R_s) (L_{g1} + L_{s1})}{C_{gs1}}}$$

$$\omega_{o,rfbn} = \sqrt{\frac{1}{(L_{g1} + L_{s1}) C_{gs1}}},$$

$$Q_{dn} = \frac{1}{(R_s || R_{fB}) + \omega_{T1} L_{s1}} \cdot \sqrt{\frac{(L_{g1} + L_{s1})}{C_{gs1}}},$$

where f_{gn} , f_{dn} , and f_{rfbn} are gate, drain, and feedback resistor noise factors, respectively and α , S , and γ are constants equal to 0.85, 4.1, and 2.21, respectively.

It is clear from (4) that, to reduce the noise figure, high quality factors of L_{s1} and L_{g1} are desired. It can also be noted that the noise factor is inversely proportional to feedback resistor R_f . In other words, weak feedback topology decreases the noise factor value while strong feedback implementation degrades the noise performance of the suggested UWB LNA.

In addition, the noise factor formula given by (4) states that the noise figure is also inversely proportional to the

transconductance of the input stage (g_{m1}). This goes along with the known fact that noise performance trades off with power consumption.

For output matching, the series resonance of the shunt peaking technique is used to match the proposed UWB LNA to the load impedance R_L while the series drain resistance R_{d2} is used to extend the output matching bandwidth.

This proposed UWB LNA (LNA1) has an operating bandwidth of 3.1-10.6 GHz. The proposed LNA2 whose schematic

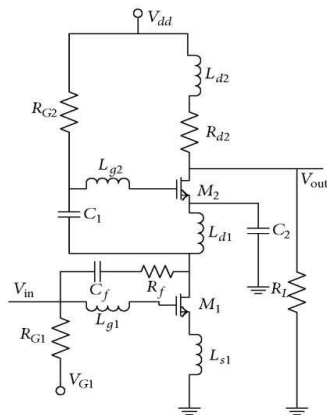


Figure : Current reuse UWB LNA (LNA1).

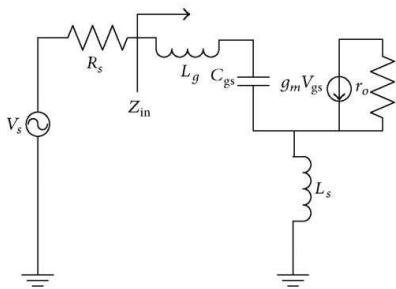


Figure : Input stage small signal equivalent circuit.

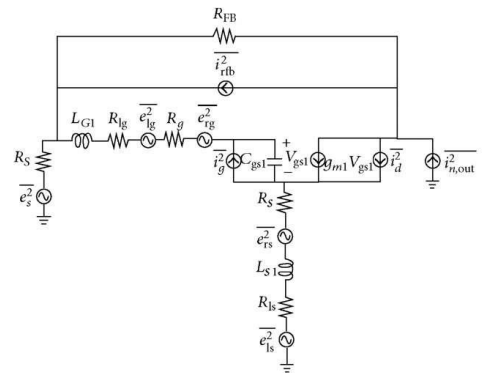


Figure : Equivalent circuit of the first stage for noise calculation.

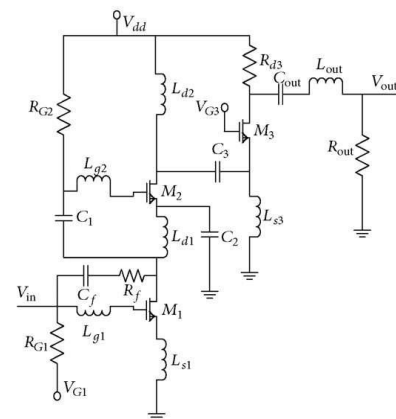


Figure : Schematic circuit of LNA2.

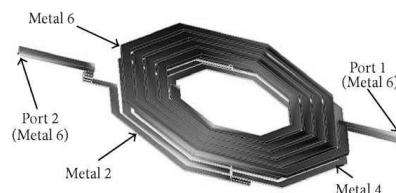


Figure: 3D view of the symmetric 3D proposed structure.

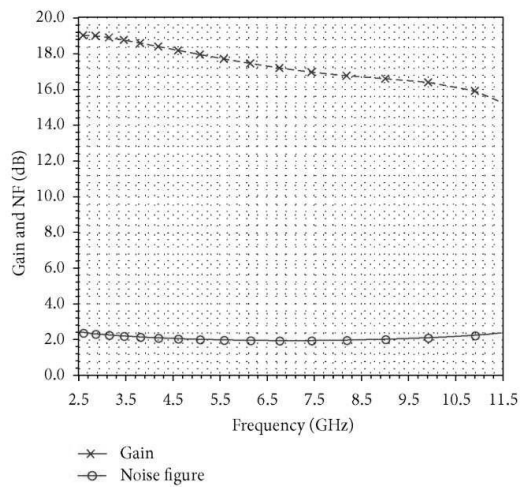


Figure : S_{21} (dB) and NF (dB) of LNA1.

circuit is demonstrated in Figure is an augmented form of LNA1. It has a more extensive working band of recurrence which broadens from 2.5 Ghz to 16 Ghz.

Info impedance match has an extraordinary imperativeness and attention particularly in wideband touchy circuits outline. Information impedance matching transfer speed is grown by the utilization of a weaker shunt capacitive-resistive sentiment circle which basically expedites quality consider decrease of the information matching circuit. Shortcoming of shunt sentiment quality not just lessens the data reflection coefficient over this wide data transmission however it additionally decreases the information side infused warm noise which diminishes the proposed LNA2 noise figure showing the improved noise exhibition of the proposed configuration.

Shunt-cresting procedure increments the low recurrence pick up and thus diminishes the increase evenness while having a wide working transfer speed. Regardless of shunt-cresting disadvantages, it mostly expedites LNA yield impedance to load matching. LNA2 transfer speed amplification and pick up levelness over its operating band of recurrence are attained through the evacuation of shunt topping. Besides the control of door cresting is utilized to improve the present reuse amplifier center addition.

For wideband yield impedance matching, an unity common entryway (C_g) matching topology notwithstanding arrangement. resonance circuit consisting of capacitor C_{out} and inductor L_{out} is used to match the LNA2 output impedance to its load (succeeding RF stage). The resistive termination R_{out} is used to control the load-output impedance match bandwidth.

A planar RF on-chip spiral inductor (L_{d1}) having an inductance of 14.5 nH and a maximum quality factor of 8.0 is needed as a load of the input CS stage to improve the current reuse stages matching. This RF integrated inductor occupies an area of $428 \mu m \times 425 \mu m$ which represents a considerable part of the UWB LNA total die area.

One of the well-known difficulties facing the development of RFICs is inductors large area relative to other passive and active components. This area problem becomes more severe with the recent intensive shrinking of active devices and competitive reduction of fabrication cost.

Inductors quality component (Q) diminishment is an additional constraining element of RFICs exhibition improvement. The lessening of inductor Q element is because of ohmic and substrate misfortunes. Ohmic misfortunes might be diminished by utilizing a high conductive metal for inductor execution. Then again putting a high resistive layer underneath the inductor can minimize the substrate misfortunes. Of late upgraded 3d structures and executions of Rf coordinated inductors are prescribed to defeat the sum of these impediments and enhance the Rf coordinated inductors exhibition.

For LNA2 circuit zone diminishment and Rf inductor characteristics change, a symmetric 3d structure for R_f joined inductor usage is prescribed to supplant the planar R_f joined inductor (L_{d1}). Comparative to the configuration of planar R_f inductor, 3d metallic structure layout ought to be attracted on a substrate to plan and test a 3d mixed inductor. 3d Rf inductors structures are chiefly consist-ing of serially joined distinctive metal layers spirals having the same current flow course. This 3d structure inductance is reliant on these diverse spirals inductances and the positive shared coupling they have.

For 1p6 M CMOS innovation which has six distinctive metal layers, the proposed symmetric 3d R_f joined inductor has a complete winding inductor on the most noteworthy metal layer (M6). 50% of the lower winding is achieved utilizing fourth metal layer (M4) to expand its inductance esteem because of the expanded common coupling. The second metal layer (M2) which is inaccessible from the top metal layer is utilized to enable the lower winding other half to decrease the parasitic parts of that 3d metal structure and increment its quality component. The recommended symmetric 3d inductor has an inductance of 14.5 nh, a quality component of 8.5, and a territory of $185 \mu m \times 165 \mu m$. 80% of planar inductor territory is safeguarded through this symmetric 3d structure while accomplishing the same inductance esteem and higher quality component.

SIMULATION OUTCOMES AND DISCUSSION

The proposed UWB LNA (LNA1 and LNA2) circuits are composed in TSMC CMOS 0.18 μm innovation process utilizing Agilent Advanced Design System (ADS). Electromagnetic reproduction is confirmed by the post-layout reenactment results which are acquired utilizing the Cadence nature. The proposed symmetric 3d structure is outlined and tried utilizing Momentum reenactment programming and checked utilizing Cadence nature's domain. The LNAs reproduction effects are given below.

(1) power Gain and Noise Figure. LNA1 has an addition of 17 ± 1.5 db as indicated in Figure. It additionally has a noise figure less than 2.3 db over its working band of recurrence (3.1-10.6 GHz).

S₂₁ (db) of LNA2 is higher than 10 db with a most extreme worth of 12 db over the wanted band of recurrence (2.5-16 GHz). This high and level increase is because of the utilization of inductive increase topping strategy notwithstanding the control of the unity increase current cut-off frequencies of LNA2. Figure shows that the proposed LNA2 utilizing the symmetric 3d Rf mixed inductor accomplishes an addition of 11 ± 1.0 db.

The proposed UWB LNA2 has an improved LNA noise exhibition. LNA2 Nf goes from 2.5 db to 3.3 db over the working data transfer capacity (2.5-16 GHz). This Nf diminishment is proficient because of the improvement of the LNA noise calculate given by (4) and the utilization of frail shunt capacitive-resistive reaction actualized over the information stage. LNA2 accomplishes a Nf less than 3.3 db over the working band of recurrence as demonstrated in Figure.

(2) input and Output Impedance Matching. LNA1 data and yield ports have exceptional matching conditions to its source and load, individually. Reproduction comes about of information and yield reflection coefficients of LNA1 are demonstrated in Figure. LNA1 has S₁₁ and S₂₂ less than -11 db and -10 db, separately, over the UWB extend of frequencies.

The proposed UWB LNA2 attains exceptional information im-pedance matching as demonstrated in Figure. Great impedance match between LNA2 and its source is obtained using the series-resonant input matching technique. The input return loss (S₁₁) is less than -7.0 db over this wide range of frequency (2.5-16 GHz).

Reference	BW (GHz)	Gain (dB)	NF (dB)	S ₁₁ (dB)	S ₂₂ (dB)
This work (LNA2)*	2.5~16	11 ± 1.0	<3.3	< 7	< 7.25
This work (LNA1)*	3.1~10.6	17 ± 1.5	<2.3	<-11	<-10
LNA-1 [1]	1.7~5.9	11.2 ± 2.3	<4.7	< 11.8	< 12.7
LNA-2 [1]	1.5~11.7	12.2 ± 0.6	<4.8	<-8.6	<-10
[2]	3~10.6	15	<4.4	<-7	NA
[12]	3.1~10.6	10.8 ± 1.7	<6	< 10	< 9.3
[13]	1~5	12.7 ± 0.2	<3.5	<-8	NA

Table: Proposed UWB LNA performance summary in comparison to recently published UWB LNAs.

Figure shows that better output impedance matching is obtained using the planar integrated inductor while simulating LNA2. Good output impedance matching of LNA2 over its operating band of frequency (2.5-16 GHz) is accomplished due to the optimization of the CG output matching stage with the aid of the output LC resonant circuit. R_{out} termination is used to widen the matching bandwidth. The output return loss (S₂₂) shown in Figure is less than -7.25 dB for LNA2 using the planar inductor while it is less than -6.0 dB for LNA2 employing the proposed 3D inductor over the desired frequency band (2.5-16 GHz).

DC Power, Reverse Isolation, and Stability. LNA1 and LNA2 consume DC power of 12.8 mW and 20 mW, respectively, from a 1.8V power source. The increased DC consumption of LNA2 is due to having enough driving bias for the CG output match stage.

Both of the proposed UWB LNA1 and LNA2 have a reverse isolation factor (S₁₂) less than -28 dB over each design bandwidth. The proposed UWB LNAs (LNA1 and LNA2) are unconditionally stable over their bandwidths.

Table shows a summary of the proposed UWB LNAs performance in comparison to other recently published UWB LNAs implemented in 0.18 μm CMOS technology.

CONCLUSION

In this paper, two different UWB LNAs were presented. LNA1 has high gain, minimized noise figure, and good impedance match over the UWB range of frequencies. LNA2 has a wide range of operating frequency (2.5 GHz-16 GHz). UWB LNA2 consists of a current reuse cascaded amplifier with shunt resistive feedback followed by a CG output stage with resistive termination. LNA2 input stage uses series-resonant impedance matching technique and employs a symmetric 3D RF integrated inductor as a load. The post-layout simulation results of LNA1 and LNA2

demonstrate the performance improvement achieved through these designs. The next step is to implement these UWB LNAs to have a comparison between post-layout simulation results and measured results.

REFERENCES

- Y. S. Lin, C. Z. Chen, H. Y. Yang et al., "Analysis and design of a CMOS UWB LNA with dual-RLC-branch wideband input matching network," *IEEE Transactions on Microwave Theory and Techniques*, vol. 58, no. 2, pp. 287-296, 2010.
- I. A. Galal, R. K. Pokharel, H. Kanay, and K. Yoshida, "Ultra- wideband low noise amplifier with shunt resistive feedback in 0.18 μ m CMOS process," in *Proceedings of the 10th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF '10)*, pp. 33-36, January 2010.
- K. Yousef, H. Jia, R. Pokharel, A. Allam, M. Ragab, and K. Yoshida, "A 2-16 GHz CMOS current reuse cascaded ultra- wideband low noise amplifier," in *Proceedings of the Saudi International Electronics, Communications and Photonics Conference (SIECPC '11)*, April 2011.
- K. Yousef, H. Jia, R. Pokharel, A. Allam, M. Ragab, and K. Yoshida, "Design of 3D Integrated Inductors for RFICs," in *Proceeding of 2012 Japan Egypt Conference on Electronics, Communications and Computers (JECECC '12)*, pp. 22-25.
- X. N. Wang, X. L. Zhao, Y. Zhou, X. H. Dai, and B. C. Cai, "Fabrication and performance of novel RF spiral inductors on silicon," *Microelectronics Journal*, vol. 36, no. 8, pp. 737-740, 2005.
- M. Niknejad and R. G. Meyer, "Analysis, design, and optimization of spiral inductors and transformers for Si RF IC's," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 10, pp. 1470-1481, 1998.
- T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, Cambridge University Press, 2nd edition, 2004.
- S. S. Mohan, M. Del Mar Hershenson, S. P. Boyd, and T. H. Lee, "Bandwidth extension in CMOS with optimized on-chip inductors," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 3, pp. 346-355, 2000.
- H. T. Friis, "Noise figure of radio receivers," *Proceedings of the IRE*, vol. 32, no. 7, pp. 419-422, 1944.
- H. Y. Tsui and J. Lau, "Experimental results and die area efficient self-shielded on-chip vertical solenoid inductors for multi-GHz CMOS RFIC," in *Proceedings of the IEEE Radio Frequency Integrated Circuits (RFIC) Symposium*, pp. 243-246, June 2003.
- H. Garcia, S. Khemchndai, R. Puidlo, A. Lturri, and J. Pino, "A Wideband active feedback LNA with a Modified 3D inductor," *Microwave and Optical Technology Letters*, vol. 52, pp. 1561-1567, 2010.