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# Reliable electronic front-end circuits for permanent, non-invasive health monitoring in biomedical wearables

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**Abstract:** Developing reliable electrical front-end circuits is crucial for biomedical wearable devices to offer long-term, non-invasive health monitoring. The digital health monitoring system's main interface with the human body is these circuits, which enable accurate bio signal acquisition, amplification, filtering, and digitisation. Thanks to advancements in energy-efficient signal processing, flexible electronics, and low-power analogue front-end (AFE) designs, modern biomedical equipment is far more efficient and simpler to wear. This project aims to develop new circuit designs that can integrate biopotential, temperature, and photoplethysmography (PPG) sensors to constantly monitor vital indicators such heart rate, temperature, oxygen saturation, and electrocardiogram (ECG) data. Efforts were made to optimise power consumption, noise performance, and signal quality in order to ensure long-term usage without frequent charging. We also take a look at several innovative materials and system-on-chip (SoC) solutions to demonstrate how they may work with skin-conformal or textile-based platforms. Modern, user-friendly, and mobile personalised healthcare apps are made possible by these front-end circuits, which offer wireless transmission and real-time data processing. The reliability and biocompatibility of the circuits are assessed for long-term usage, highlighting their significance in preventative and remote health monitoring systems.

**Keywords:** electronic, front-end circuits, non-invasive, health monitoring, biomedical wearables

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## INTRODUCTION

A new age in biomedical engineering has begun with the introduction of flexible electronics, which has had a profound influence on the creation of efficient front-end circuits for wearable devices that continuously and noninvasively track health. More and more, people are looking for pleasant, long-term physiological monitoring technology that can connect with their bodies flawlessly, and this demand is driving these improvements. The biocompatibility, comfort, and form factor of traditional, rigid electronics can be compromised with prolonged usage, particularly in dynamic settings(Barold, S. S. 2003). In contrast, mechanically compliant, lightweight, conformable, and stretchy flexible electronics are ideal for skin-contacting wearable healthcare equipment. Acquiring, amplifying, filtering, and converting digital signals to analogue ones before processing or transmission is a crucial function of these systems' front-end circuits. If we want these circuits to work reliably and efficiently while consuming little energy, we need to use cutting-edge materials science, device engineering, and circuit design techniques to construct them on flexible substrates. These front-end circuits may now be housed on biocompatible, flexible substrates like as polyimide, thermoplastic polyurethane (TPU), or polyethylene terephthalate (PET). They can also be used with organic semiconductors, nanomaterials, printable electronics, thin-film transistors, and more. These circuits are often the basis for biosensors that monitor temperature, blood pressure, $SpO_2$, hydration,

glucose concentration, electrocardiogram (ECG), electromyogram (EMG), and electroencephalogram (EEG) (Korf, J. 1996).

The confluence of flexible electronics, the Internet of Things (IoT), and artificial intelligence (AI) is allowing wearable health monitoring devices to become smarter, more autonomous, disease-detecting, and healthcare intervention-specific. Power consumption is a major issue for all applications, but especially for continuous monitoring systems. This highlights the need to investigate energy harvesting methods and create ultra-low-power circuits. To address these concerns, researchers are developing innovative analogue front-end (AFE) topologies, efficient rectifiers, low-leakage transistors, and low-dropout regulators that can dependably handle low voltages and currents without signal deterioration. Data may be securely and efficiently transmitted from these front-end circuits to smartphones or cloud-based health platforms thanks to recent developments in wireless communication circuits, such as those based on BLE, NFC, and body-coupled communication(Zhang, Y.-T. 2006). Flexible front-end circuits must be protected from biocompatibility issues, mechanical stress, and moisture using system-level packaging solutions and encapsulation techniques. Among the many possible medical applications of flexible electronics-based front-end circuits are medical-grade monitoring of chronic diseases, rehabilitation, analysis of sleep, evaluation of mental health, and care for both the young and the elderly(M.-K. 2005). Not only do these devices put patients more at ease due to their covert design, but they also aid physicians in making more precise diagnoses and developing more effective treatment programs through the continuous streams of high-fidelity data they provide. Teams of experts from many fields are working together to find solutions to issues related to signal quality, mass manufacturability, miniaturisation, and long-term stability. These teams include electrical engineers, materials scientists, biophysicists, and medical specialists. In order to promote their increased use in healthcare markets, innovative fabrication techniques including as 3D printing, inkjet printing, and roll-to-roll processing are being employed to mass-produce flexible front-end circuits at reduced costs (Taccini, N. 2005).

Integrating machine learning algorithms at the edge of these flexible systems significantly enhances the functional capabilities of wearable health monitoring. As a result, anomaly detection, context-aware decision-making, and real-time signal classification are all made possible. The design approach is now taking ethical and privacy considerations into account alongside security and the proper use of user data. Finally, the development of practical front-end circuits built on flexible electronics has been a huge step forward in the race for continuous, noninvasive health monitoring. Innovative low-power circuit design, wireless connectivity, clever signal processing, and flexible materials have all found common ground in these circuits (Verma, N. (2016).

## METHODOLOGY

For biomedical wearables to provide continuous, non-invasive health monitoring, a methodical and interdisciplinary strategy is needed to integrate materials science, electrical circuit design, signal processing, and biomedical engineering into the development of effective front-end circuits based on flexible electronics. We review the current state of the art in biomedical front end circuit design, flexible electronics, and thin-film transistors (TFTs) by reviewing the relevant literature. This review will assist you in identifying performance gaps, limits, and opportunities while building flexible circuits for wearable

health monitoring devices. We will now move on to the important task of selecting and researching the appropriate flexible materials, including oxide-based semiconductors (IGZO), biocompatible substrates (polyimide or PDMS), and other components. The selection of these materials is based on their mechanical, electrical, and physiologically advantageous characteristics. For the purpose of determining their suitability for use in wearable applications, experimental research and simulations will be used to evaluate the mechanical flexibility and electrical performance of these materials. The next step is to build and model the front-end circuits, which include signal acquisition modules, pre-processing blocks (such filters and amplifiers), and analog-to-digital converters (ADCs). Minimal power consumption, excellent signal quality, and little noise will characterise these circuits when they undergo extensive fine-tuning. Using noise-reduction techniques like chopper-stabilized circuits and low-power operational amplifiers, we can accurately acquire weak physiological data including ECG, EMG, temperature, and oxygen saturation.

## RESULTS

An oxide TFT model bootstrapping circuit has never been observed or simulated previously by Cadence. By adjusting the φ1 and φ 2 clock frequencies, you may test the circuit up to 1 MHz. These two clocks may be supplied to the entire system-on-chip by the Pseudo-CMOS BS RO, as shown in Figure 1. This circuit allows for the generation of full rail-to-rail timing signals using just a 3 V power supply.

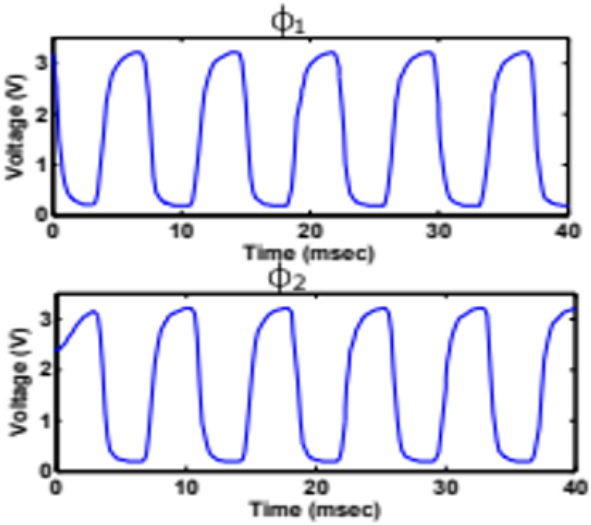


**Figure 1: The ring oscillator simulation results for the creation of two inverted clock pulses (a) φ1 and (b) φ2.**

In Fig. 2, we can see the bootstrapping circuit's simulation results for various clock frequencies and a 2 Mı load. It takes around fifty-five hundredths of a second to settle.

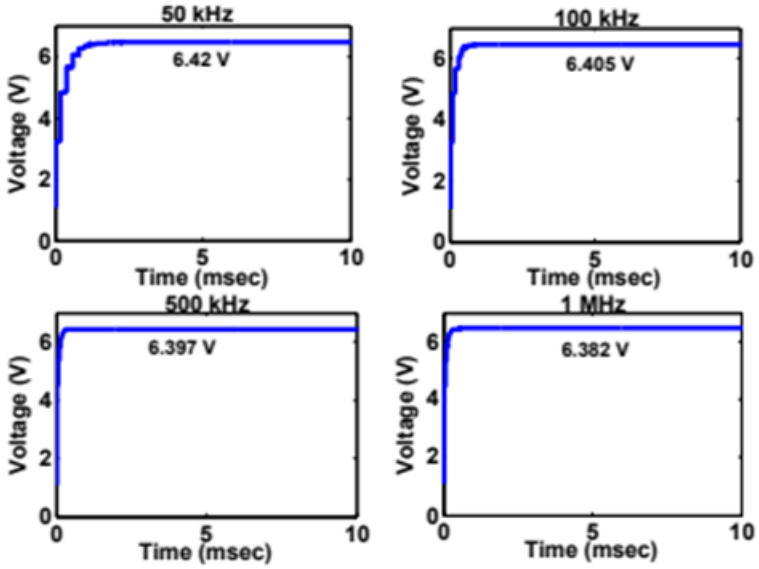


**Figure 2: Simulation results for a bootstrapping circuit with an input voltage of 3 V and a load of 2 MΩ at clock frequencies of 50 kHz, 100 kHz, 500 kHz, and 1 MHz**

Both the parasitics in the transistors and the finite non-zero on-resistance of the switches are to fault for this. Typically, the on resistance of a TFT is directly proportional to the time it takes for it to settle. A wide TFT results in charge injection that is not insignificant, whereas a small TFT provides a high on-resistance, supposing the channel length stays the same. A compromise between the two criteria was used to establish the proper size of the TFTs in order to complete the transition. It is evident that when the input voltage is 3 V, the output voltage is higher than 5 V. Regardless of the clock frequency, the output stays constant at around 6.4 V when subjected to a 2 MΩ loading condition. This continuous voltage may be used as VDD by the remaining low power signal processing blocks in a system-on-a-chip configuration. Moreover, the circuit is perfect for versatile biomedical applications due to its exceptionally low power consumption of 24.9 µW, even with a 2 MΩ load. A PVT study was conducted using 180 nm CMOS technology to assess the resilience of the bootstrapping circuit. The results show that relative to process, voltage, and temperature, there is a 2.3% variance, a 1.2% variation, and a 10% variation, respectively. In the absence of oxide TFT models for statistical simulations, this investigation was performed using NMOS devices. So, it's reasonable to assume that this circuit is ideal for real-world applications.

The output voltage of the suggested circuit is shown in Fig. 3 for 2 MΩ and 5 MΩ loading situations, where the input voltage ranges from 2 to 10 V. In Table 1, we can see the response of the circuit under various loading scenarios.

**Table 1: Various loads' output voltage and current when fed a 3 V input**

| S. No. | Loads (MΩ) | Voltage (V) | Current (µA) |
|---|---|---|---|
| 1 | 1 | 5.2 | 5.2 |

| | | | |
|---|---|---|---|
| 2 | 2 | 6.4 | 3.2 |
| 3 | 5 | 7.9 | 1.58 |
| 4 | 10 | 8.3 | 0.83 |
| 5 | 25 | 8.8 | 0.352 |
| 6 | 50 | 8.99 | 0.179 |

Due to the less-than-ideal characteristics of switches, including their threshold voltage drop and restricted on-resistance, the output voltage is lower than 3*VDD. Another way that the load resistance dictates the output voltage is... The device has the capability to produce a voltage of up to 3*VDD when tested with a 50 MΩ load. This circuit can power other analogue pre-processing circuits that employ oxide TFTs while using very little power. A micrograph of the bootstrapping circuit is shown in Figure 3.4. When achieving the desired voltage by connecting many batteries in series, the bootstrap circuit takes up only around 25 (μm)2 in space, which is far smaller than the printed batteries. The system can be condensed with the help of this circuit.

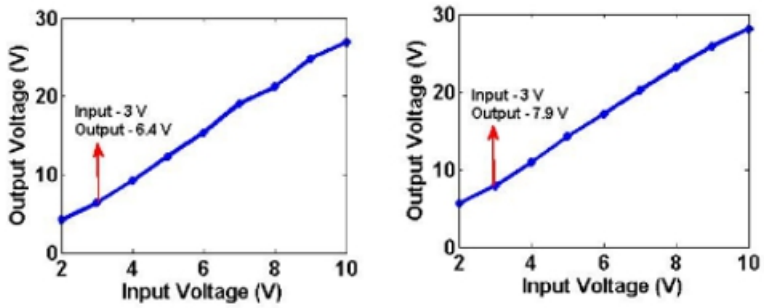


**Figure 3: Bootstrapping circuit simulation results with varying loading circumstances (a) 2 MΩ and (b) 5 MΩ at a clock frequency of 1 MHz.**

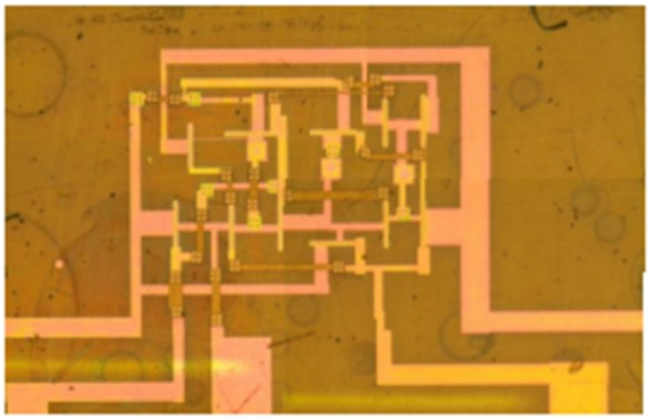

**Figure 4: Micrograph following a-IGZO TFT boostrapping circuit construction.**

**Optoelectronic ring oscillators**

Figure 3.5(a) shows that the suggested Bootstrapping circuit may be implemented by using the suggested Ring Oscillators (RO) to create the clocks (φ1 and φ2). This section will go over four distinct RO implementations that make use of IGZO TFTs: Diode connected load, Capacitive bootstrapping (BS), Pseudo-CMOS, and PseudoCMOS bootstrapping. Within a cadence setting, these topologies have been modelled using in-house IGZO TFTs under comparable circumstances and varying power sources (10 V, 15 V, and 20 V). Similarly, when tested with thin-film batteries that are supplied with voltages ranging from 3 to 9 volts, the results that were mentioned hold true. Many reports of ROs using a-IGZO TFTs have been published up to this point. The output voltage swing becomes worse when using several stages in cascade since there is no complementary device and there is inadequate noise buffer. Excessive static electricity is also used by this process. One possible monotype TFT-based solution to the output swing and other concerns is depletion load dual gate dual Vth TFTs. Due to the need for specialised TFT properties, extra masks, and manufacturing processing procedures, the approaches have limited practical use. Using amorphous oxide semiconductors (AOS) with the properties of complementary metal-oxide semiconductors (CMOS) is difficult. Furthermore, n-type AOS and p-type organic/carbon nanotube TFTs can coexist in specific hybrid designs. The production of these hybrid structures is complex and costly due to a number of manufacturing factors. It should be mentioned that comparing the performance of the circuits becomes considerably more challenging when using n-type oxide TFTs alone, as this technology is not standardised internationally like ordinary CMOS. Various Fabs use a wide variety of processing methods, device topologies, and materials when it comes to this technology. As a result, it is not always easy to determine which on-chip clock generator (RO) architecture is most suited to a particular application's performance requirements. In this work, the key topologies that were studied for RO implementation were diode-connected load, hybrids of the two, and pseudo-CMOS with capacitive bootstrapping. With voltages ranging from 10 to 20 V, all of the circuits were simulated using our proprietary TFT software. In this paper, we compare two inverter topologies that were used under the same conditions: a-IGZO TFTs and ROs. After this, we delve even further into the quantifiable outcomes of these ROs.

**Circuit Description**

A ring oscillator, made up of an odd number of inverters linked in a ring arrangement, is able to generate oscillations. All of the designs demonstrated in this paper have been implemented utilising a-IGZO TFTs, which are essentially n-type, as opposed to the traditional CMOS-based RO that uses both PMOS and NMOS transistors. Considering the system's size constraints, this study investigated a 5-stage RO that relies on an inverter (see Fig. 3.5). The ring oscillator is governed by this inverter architecture in terms of overall performance. Therefore, we will begin by discussing several inverter methods that solely rely on n-type transistors.

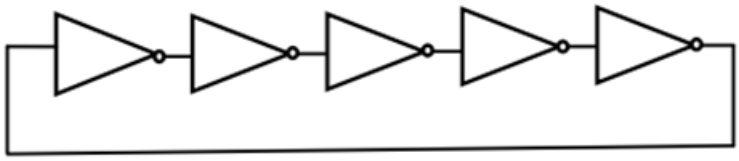

**Figure 5: A five-stage oscillator for rings.**

**1. Inverter with diode connected load:** You can see the circuit diagram with the diode load inverter in Figure 6(a). In this case, the channel lengths of M1 and M2 are identical.

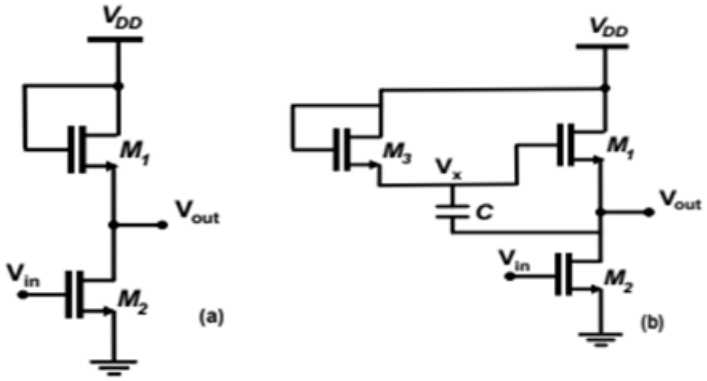


**Figure 6: A diode-connected load and a capacitive bootstrapping load are both present in the inverter**

For voltage swing to be encouraged, WM2 > WM1. Turning down the input voltage (Vin) effectively turns off M2 and results in nearly little current flowing through the device. The output voltage, Vout, is thus approaching VDD-Vth1. Because a voltage drop across M1 occurs with a rise in drain current, Vout decreases as Vin increases. In this case, we may use equation (1) to find Vout.

$$V_{out} \approx V_{DD} - \frac{1}{g_{m1}} I_D \qquad 1$$

This topology does not allow for full swing. Figure 3.6(a)'s low frequency gain may be calculated using (2), which is derived from tiny signal analysis.

$$A_v = \frac{g_{m2}}{g_{m1} + g_{ds1} + g_{ds2}} \qquad 2$$

If $g_m >> g_{ds}$, then

$$A_v \approx \sqrt{\frac{W_2}{W_1}} \quad 3$$

Table 2 shows that in order to achieve a high gain, which is defined as a sharp transition between the VOH and VOL voltage transfer characteristics, a wide driver transistor is needed. This wide transistor then leads to large parasitics, which reduce the operation frequency mainly because of the miller capacitance (Cgd of M2) formed by the extensive overlap between the gate and drain.

**2. Inverter with capacitive bootstrapping load:** Capacitive bootstrapping load is another possible topology for a-GIZO TFTs, as demonstrated

**Table 2: Various inverter topologies and their corresponding transistor dimensions**

| S. No. | Inverter Topology | Transistors | W (µm) | L (µm) |
|---|---|---|---|---|
| 1 | Diode connected | M1 | 20 | 20 |
| | | M2 | 320 | 20 |
| 2 | BS | M1, M2 | 160 | 20 |
| | | M2 | 20 | 20 |
| 3 | Pseudo CMOS | M1, M2 | 160 | 20 |
| | | M3 | 20 | 20 |
| | | M4 | 20 | 20 |
| 4 | Pseudo-CMOS BS | M1, M2 | 160 | 20 |
| | | M3 | 20 | 20 |
| | | M4 | 20 | 10 |

Shown in Figure 6(b). The source and gate electrodes of transistor M1 are connected in this circuit with a

bootstrapping capacitor C. To make sure the bootstrapping works, the value of C should be higher than the parasitics introduced by the TFTs in the circuit. Since no low-impedance channel is available to drive current in this architecture, M3 is constantly in the cut-off state.

M2 conducts and Vout reaches VOL when input is high.

$$V_{out} = V_{OL} \quad 4$$

The voltage at the Vx node is as follows: (5).

$$V_x = V_{DD} - V_{GS_3} \approx V_{DD} \quad 5$$

M2 turns off and Vout rises approaching VDD as input drops. This is because bootstrapping:

$$V_x \approx 2V_{DD} - V_{GS_3} - V_{OL} \quad 6$$

This architecture is commonly employed to enhance the VOH by elevating the gate voltage of the load TFT (M1) beyond VDD. The bootstrapping capacitor and the aspect ratio of the transistors determine the operating frequency for a certain technology. This design has the drawback of having VOH ≈ VDD but low VOL > 0 V.

**3. Inverter with pseudo-cmos load:** The pseudo-CMOS inverter, seen in Figure 7(a), is the third topology. The CMOS inverter's behaviour may be mimicked by this arrangement. The CMOS inverter behaviour may be reproduced by adding two more TFTs, M3 and M4, which apply inverted signals to M1 and M2. M2 is turned off and M1 is turned on when the input is low. Equation (13) gives the output voltage Vout.

$$V_{out} \approx V_{DD} - 2V_{th} \quad 7$$

Vout ≈ VSS when M1 is turned off and M2 is turned on in response to a high input. By turning M2 on and M1 off, respectively, this inverter increases the output swing, which is largely VOL. Compared to bootstrapping RO, which uses smaller dimensions for M3 and M4 in Fig. 3.7(a), this helps to lower the static current via M1 and M2 branch, leading to low power consumption.

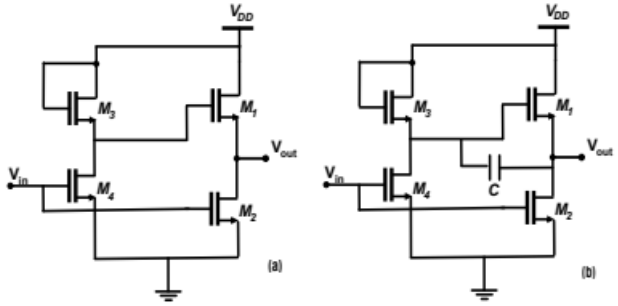


**Figure 7: Both (a) pseudo-CMOS and (b) pseudo-CMOS bootstrapped configurations were used to**

**create the circuit design**

**4. Pseudo-cmos bootstrapped inverter:** "Pseudo CMOS" was the advantages of bootstrapped inverters and pseudo-CMOS are combined in bootstrapped inverters, as shown in Figure 3.7(b). By adding two more transistor field-effect transistors (TFTs) M3 and M4 in front of the load TFT (M1), the Pseudo-CMOS design may increase VOL and decrease static current M2 through the driving TFT, simulating the action of a CMOS inverter. The bootstrapped capacitor allows for an increase in VOH. Upon rising from a low input state, M1 is disabled and M2 is enabled due to the inverted gate signal. By connecting the output node to VSS ≈ VOL ≈ 0, this may be achieved. As input levels drop, M1 becomes active and M2 becomes inactive. Bootstrapping with C also raises M1's gate voltage in response to an increase in the output voltage. Using the bootstrapped high gate voltage at M1, it is feasible to get VOH closer to VDD. To clarify, the advantages of both the Pseudo-CMOS and Capacitive BS methods are maintained, with VOH = VDD and VOL≨ 0. You can get almost full output voltage swing with this design, and you won't have to compromise on frequency or power.

The proposed building blocks have been successfully included into the biomedical acquisition front-end in this study. We used pseudo-CMOS BS RO after comparing it to other ROs employing oxide TFT technology. To reduce the system's space needs and merge it onto a single chip, this study initially introduces the bootstrapping circuit. The pre-amplifier, which boosts the weak signal, is the second critical component. The pre-amplifier features a simple design to minimise the system's total footprint. The complex circuit's production is also very important because of the low yield; this is a big deal since oxide TFT is a brand new technology. Consequently, the intended application is achieved in this study by means of a simple positive feedback amplifier design. Another essential component is the LPF (antialising filter). SC As a first step, this study proposes Sallen-and-Key LPF (up to sixth order) for component removal. The measured findings of this filter have also been mentioned in the thesis. At that point, the ADC becomes an integral part. This is the most important part of the biomedical analogue front-end. At its heart, an ADC is a comparator. Five different types of comparators are suggested in this research. There is a proposed new class of dynamic comparators. The most suitable comparator has been selected from among five alternates. Two different kinds of ADCs are now in the works. Two types of Δ-΄Y ADCs are available to you: an active one and a passive one. When compared to state-of-the-art investigations, the findings of both ADCs' simulations show improved ENOB and FOM. Finally, the biological front-end with the existing printed battery was formed by combining the suggested blocks, which included an active Δ-ξ ADC, a 2nd order SC Sallen-and-key LPF, a bootstrapping circuit, and a pseudo-CMOS BS RO. With an ENOB of 8.9 bits, our simulation results for the analogue front end significantly outperform the state-of-the-art.

## CONCLUSION

Biomedical wearables that provide long-term, non-invasive health monitoring rely heavily on robust electrical front-end circuits. These circuits allow for the conversion of biological impulses into digital form, which guarantees the continuous, accurate, and noise-free collection of physiological data. Achieving long-term, unobtrusive monitoring with wearable healthcare equipment requires front-end circuit designs that prioritise power economy, miniaturisation, signal integrity, and user comfort. The evolution of integrated system-on-chip (SoC) solutions, flexible substrates, and low-power analogue front-end (AFE) designs has resulted to smaller, more energy-efficient, and physiologically sensitive wearable devices. These

advancements provide essential features of contemporary personalised care, such as continuous remote patient monitoring, early illness identification, and real-time diagnostics. Wearability and durability are both improved by including biocompatible and flexible materials into the device. New directions in R&D have shown encouraging results despite obstacles such energy constraints, signal interference, and motion artefacts. For biomedical wearables to be scalable and used in the real world, these circuits must be reliable and function well. The development of more reliable electronic front-end circuits will have far-reaching consequences for the future of healthcare prevention, chronic illness management, and mobile health technology, giving people more agency over their own bodies.

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