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Short Channel Effects in Nanoscale Fully Depleted Double-Gate SOI Mosfets

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Abstract – In this paper is discussed how the short channel behavior in sub 100nm channel range can be improved by inducing a step Surface potential profile at the back gate of an asymmetrical double gate (DG) silicon-on –insulator (SOI) metal-oxide –semiconductor field-effect-transistor (MOSFET) in which the front gate consists of two materials with different work function.'

INDEX - PD and FD SOI devices, Short Channel Devices, Short Channel Effects

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INTRODUCTION

DOUBLE-GATE (DG), silicon-on-insulator (SOI) technology has been regarded as another main stream technology for sub-100-nm CMOS very large-scale integration (VLSI) owing to its advantages in reduced short channel effects. Many aspects of DG SOI devices have been studied. For DG SOI CMOS devices, the gate misalignment has a large effect on device performance. In this paper we have studied about PD and FD double gate SOI mosfets. There are many short channel effects as we go on decreasing size of a mosfets. Different short channel effects and how to avoid these effects have been studied.

PD AND FD SOI

The two types of SOI devices, PD-SOI and FD-SOI, refer the character of the depletion in the gate region. In partially depleted processes, the thickness of the active silicon layer is greater than the depletion width under the gate, leaving a neutral region that extends down to the buried oxide insulation layer. This neutral region gives PD-SOI devices unique characteristics caused by the so called floating body effects (FBE). These "parasitic" effects can be used to increase the operating frequency of the devices. On the other hand, substantial efforts are needed when transferring bulk CMOS designs to PD-SOI to allow for these effects. In FD-SOI devices, the active silicon layer is thin enough that the depletion width extends completely to the underlying oxide layer. Because of this the sub threshold slope v of the device is steeper, nearing the theoretical value of 63 mV/dec. This characteristic allows reducing the leakage current at the same threshold voltage (Vth), reducing Vth, or a combination of the two. At the same time the 1/f noise can be reduced by more than one decade and the temperature characteristic of Vth is improved to approximately 0.8 AmV/degree K, which provides the basis for the high temperature capability of FD-SOI. FD- SOI does not have the FBE of PD-SOI, which allows transfer- ring designs from bulk processes in a more straightforward manner. In production, FD-SOI devices require carefully controlling the silicon thickness, with values in the order of 50 nm. The electrical parameters of the device are dependent on this thickness. Very high uniformity is required. This presents a major challenge. Only more specialized semiconductor production facilities have announced FD-SOI. PD-SOI devices, on the other hand, can be manufactured on standard bulk CMOS production lines.

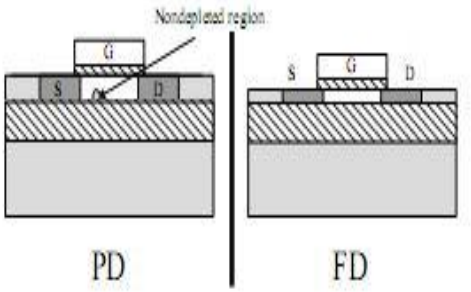

Fig. Cross section of a partially and a fully depleted SOI MOSFET device.

SHORT CHANNEL DEVICE

The design of high density chips in MOS VLSI technology requires that the packing densit y of MOSFETS used in the circuits is as high as possible, that the size of transistors are as small as possible. The reduction of size is commonly referred to as scaling. There are two basic types of size reduction

strategies: full scaling and constant voltage scaling. Both scaling gives short channel devices. A MOS transistor is called a short channel device if its channel length is on the same order of magnitude as the depletion region thickness of the source and drain junction. Alternatively, a MOSFET can be defined as a short channel device if the effective channel length Leff is approximately equal to the source and drain junction depth xj.

THE EFFECT OF SHORT CHANNEL ON NANOSCALE SOI MOSFETS

Double gate silicon-on-insulator (DG SOI) devices have recently been of great interest, particularly for the investigation of sub-10nm field-effect transistor [1]-[3]. As the channel length is reduced from one transistor generation to the next, the susceptibility of the transistor to short- channel effects (SCE) is monitored in several ways such as threshold voltage (VTH) roll-off, sub- threshold voltage swing, and the drain induced barrier lowering, the channel length decreases and becomes crucial in deep-sub micrometer technologies. As an indicator of these short channel effects, the threshold voltage and sub-threshold voltage swing has been extensively investigated [4]- [7]. Some other short channel effects are: punch through, pinholes and oxide breakdown, hot carrier injection, electro migration electrostatic discharge and electrical overstress. In order to maintain a tolerable degree of short channel effect [8], it becomes necessary to reduce the SOI film thickness. Reducing the SOI film thickness causes a high electric field in the perpendicular direction to the Si/SiO2 interface, strongly confining charge carriers in the channel. Several interesting models have been proposed for the classical (i.e., without quantum effects) drain current [9]-[11]. Carrier quantization effects have been considered for the first time in [12]. Therefore, classical models that disregard these effects are no longer suitable for describing sub 10nm MOSFETs. Therefore, we use quantum mechanical transport models for n-channel MOSFETs based on the self-consistent Schrödinger and Poisson equations for the simulation of short channel effects on the performance of DGMOSFET. In addition to it, the model is continuous over all gate and drain bias ranges, which makes it very suitable to simulate novel silicon transistor structures. Channel length reduction to sub-100 nm lengths leads to two important short channel effects: (i) threshold voltage roll-off and the drain induced barrier lowering (DIBL). A number of solutions have been proposed to minimize the short channel effects (SCEs) such as thin-body single material gate (SMG) silicon-on-insulator (SOI) metal–oxide–semiconductor field- effect-transistors (MOSFETs), double material gate (DMG) SOI MOSFETs and double gate (DG) SOI MOSFETs.(13,14) Recently, it has been shown that by replacing the single material gate of the SOI MOSFETs by a double material gate, the short-channel effects can be further controlled.(15) In the DMG SOI MOSFET, the gate is made of two materials with different work functions to introduce a potential step in the channel region.(16) As a result, the channel potential minima on the source side is unaffected by the drain voltage variations resulting in improved SCEs in the DMG SOI MOSFETs.(17,18) The primary objective of this letter is to demonstrate that if the double material gate concept is applied to the front gate of the DG SOI MOSFET, due to a strong coupling between the front and back gates, a step potential can be induced at the back gate even without having to use a double material for the back gate. Consequently, due to the induced step potential at the back gate, the double material double gate (DMDG) SOI MOSFET will have significantly improved gate control over the channel region leading to the diminished SCEs. Using two-dimensional simulation (19) we demonstrate that even for sub-100 nm channel lengths, the DMDG SOI MOSFET exhibits the desirable threshold voltage roll-up and diminished DIBL as compared with the DG SOI MOSFET due to the induced step potential at the back gate. Schematic cross- sectional views of both the asymmetrical DG and DMDG SOI MOSFETs are shown in Fig.

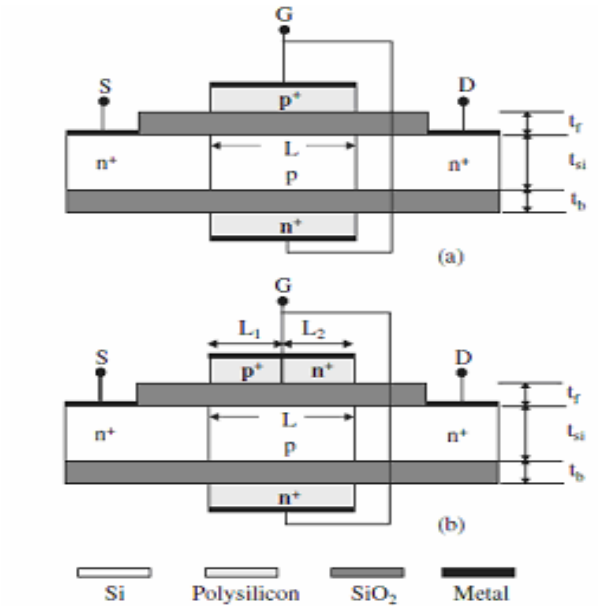

Fig. Cross Sectional view of (a) DG SOI MOSFETS and (b) DMDG SOI MOSFETS

The asymmetrical DG SOI MOSFET consists of a front p+ poly gate and a back n+ poly gate. In the case of the DMDG SOI MOSFET, the front gate consists of dual materials M1 (p+ poly) and M2 (n+ poly) of lengths L1 and L2 respectively, while the back gate is an n+ poly gate. In our simulations, the silicon thin-film thickness (tsi) is 12 nm, the front-gate oxide (tf) and the back- gate oxide (tb) thickness is 2 nm. The doping in the p-type body and n+ source/drain regions is kept at 1X1015 and 5 X1019 cm3 respectively. It can be observed that the DMDG structure exhibits a step in the surface potential profile at the front gate as well as at the back gate. The step, which is quite substantial in the front gate surface

potential, occurs because of the difference between the work functions of n+ poly and p+poly.3) Though the back gate in DMDG structure consists of a single material (n+ poly), an induced potential step can be seen at the back gate when the silicon film thickness is thin due to the coupling between the front channel and back channel. The back gate surface potential profile plays a dominant role in deciding the threshold voltage of an asymmetrical DG SOI MOSFET and due to the presence of the induced step profile at the back gate, the short channel behavior of this structure is expected to improve as discussed below. The short channel behavior of the DG and the DMDG SOI MOSFET.

CONCLUSION

In this paper we have studied different short channel effects. Then we find out the ways how to decrease these effects. Different ways are there to diminish these effects. By reducing these short channel effects we can scale down the device geometry without device performance degradation.

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