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An Investigation of Electric Power Factor a Static Correction: Converter Utilizing AC/DC Handling Techniques

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Abstract – Majority of the applications involving electronic circuitry such as those used in automotive applications and battery chargers require a regulated DC supply. Since AC supplies are more commonly available, a suitable AC-DC converter becomes mandatory for such applications. These AC-DC converters involve a number of non-linear devices which reduce the system power factor and introduce harmonics in the power system leading to adverse effects. Hence it is essential to use a suitable power factor correction technique to condition the supply current. This paper presents a comparative analysis of three such active power factor correction topologies. Simulation studies have been carried out using MATLAB/SIMULINK.

The flyback converter type single-stage converter and a half wave rectifier with time-multiplexing control (TMC) for power factor correction is proposed. It has the advantage of better magnetic core utilization and better performance for high power applications. The major portion of the input is transferred to the load through ac-dc conversion. And the part of the input power is delivered to the auxiliary output through the flyback conversion and stored in the capacitor. The voltage ripple of the main output can also be reduced. With TMC the power processes can be achieved by single transformer to reduce the cost and the size of the converter. The simulation result of the proposed converter presents, simplicity, high power factor with low cost and size.

A new parallel-connected power flow technique is proposed to improve the input power factor with simultaneously output voltage regulation taking consideration of current harmonic standards. Paralleling of converter modules is used in medium-power applications to achieve the desired output power by using smaller size of high frequency transformers. A parallel-connected interleaved structure offers smaller passive components with less loss in continuous conduction inductor current mode and also reduces the volt-ampere rating of resonant (DC/DC) converter. MATLAB/SIMULINK is used for implementation and simulation results show the performance improvement.

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INTRODUCTION

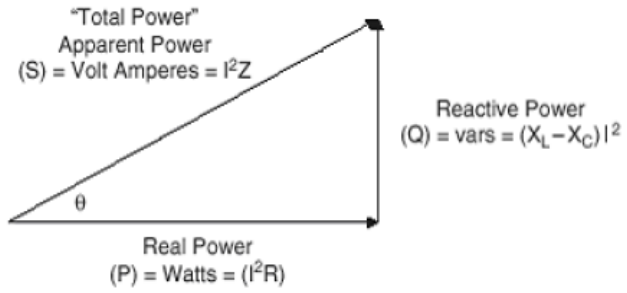
The attention devoted to the quality of the currents absorbed from the utility line by electronic equipment is increasing due to several reasons. In fact, a low power factor reduces the power available from the utility grid, while a high harmonic distortion of the line current causes EMI problems and cross-interferences, through the line impedance, between different systems connected to the same grid. From this point of view, the standard rectifier employing a diode bridge followed by a filter capacitor gives unacceptable performances. Thus, many efforts are being done to develop interface systems which improve the power factor of standard electronic loads.

An ideal power factor corrector (PFC) should emulate a resistor on the supply side while maintaining a fairly regulated output voltage. In the case of sinusoidal line voltage, this means that the converter must draw a sinusoidal current from the utility; in order to do that, a suitable sinusoidal reference is generally needed and the control objective is to force the input current to follow, as close as possible, this current reference.

Improved PF by means of a PFC front-end must also be achieved with high efficiency of the PFC stage to maintain the same or better overall system efficiency. For universal-mains-input power supplies, this high-efficiency performance must be maintained across the full AC line range to meet thermal constraints and

avoid power derating at the AC line extremities. The industry has recognized that much electronic equipment the full rated load for a large proportion of its operating life. Therefore, high-efficiency performance is being mandated across the full load range, down to 25% load, through the same ENERGY STAR and other initiatives. Many systems are also demanding better power-supply efficiencies in the 0 to 25% load range to meet stringent system-level power-consumption requirements in sleep/standby/idle modes. And of course, power supplies for computing and consumer applications have and always will be severely cost-challenged, requiring cost-effective solutions to deliver both improved PF and efficiency.

Power Factor Correction (PFC) technique continues to be attractive research topic with several effective regulations being reported. Conventional cascade of two stage topology can achieve good performance such as high power factor and low voltage stress, but it usually suffers from high cost and increased circuit complexity. Many single-stage PFC AC/DC converters have been proposed that can be applied cost-effectively. However, it's well known that in single stage topologies, the voltage across the bulk capacitor cannot be controlled well due to the fact that only one switch and control loop are used. Moreover, the storage capacitor voltage varies widely with the input voltage and load variation, especially



When the PFC operates in DCM mode while DC/DC stage operates in CCM mode. Finally, the storage capacitor voltage will increase to be unbearable under light load condition.

POWER FACTOR CORRECTION TECHNIQUES

Power factor is defined as the ratio of the real power drawn by the load to the apparent power in the circuit. Most commonly encountered loads are inductive (linear loads) in nature and hence draw lagging current resulting in reduced values of power factor. Non-linear loads such as rectifiers distort the supply current waveform and also lower the power factor to much less than unity. Hence it is necessary to use a suitable power factor correction technique to counteract the distortion and to improve the power factor.

Power factor correction topologies can be classified into:

1. Passive Power factor correction
2. Active Power factor correction

Elements in conjunction with active switches, such as IGBTs, MOSFETs and thyristors which are switched at a desirable predetermined frequency. This results in source current shaping and improves the system power factor, in addition to providing a controllable output voltage. Based on the frequency of switching of the active devices involved, active power factor correction can be classified as:

1. Low Frequency active power factor correction
2. High Frequency active power factor correction

In general, high frequency active power factor correction is preferred due to slow regulation of output voltage and the large size of reactive elements in low frequency active power factor correction topologies.

SINGLE PHASE ACTIVE POWER FACTOR CORRECTION

Conventional ON-line power converters with diode-capacitor rectifier front-end have distorted input current waveform with high harmonic content. They cannot meet the European line-current harmonic regulations defined in the IEC 1000-3-2 document nor the corresponding Japanese input-harmonic current specifications. To meet the above norms, it is to add a power factor corrector of the isolated dc/dc converter section of the switching power supply. So again another dc/dc converter is needed for output voltage regulation. So these two converters are needed for single-phase active power factor correction for the requirement of high input power factor and tight output regulation. There are two techniques for single-phase active power factor correction:

1. two-stage scheme
2. single-stage scheme

A. Two-Stage Approach of Active Power Factor Correction

Two-stage approach is commonly used approach in high power applications. the block diagram of two stage pfc converter is shown in figure 1 in this approach, there are two independent power stages. the front-end of pfc stage is usually a boost or buck-boost (or flyback) converter. The dc/dc output stage is the isolated output stage that is implemented with one switch, which is controlled by an independent pwm controller to tightly regulate the output voltage. the two-stage scheme is a cost-effective technique in high power applications; its cost-effectiveness is diminished in low-power applications due to the additional pfc power stage and control circuits.

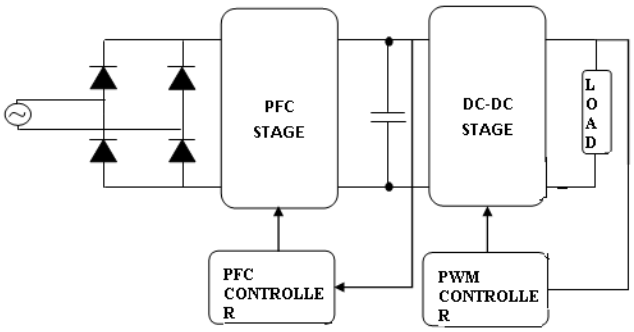


Fig. 1 : Block diagram of two stage PFC converter

B. Single- Stage Approach of Active Power Factor Correction

A single-stage scheme combines the PFC circuit and DC/DC power conversion circuit into one stage. A number of single-stage circuits have been reported in recent years. Figure 2 shows the block diagram of single-stage approach. Compared to the two-stage scheme, the single-stage approach uses only one switch and controller to shape the input current and to regulate the output voltage. Even though for a single-stage PFC converter, attenuation of input-current harmonics is not as good as for the two-stage approach. But it meets the requirements of IEC 1000-3-2 norms. Again it is cost effective and compact with respect to two stage approach.

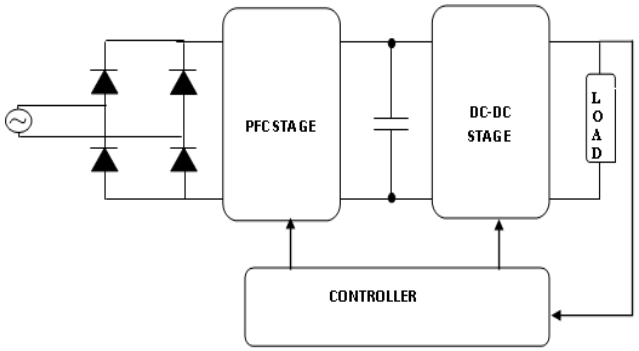


Fig. 2: the Block Diagram of Single-Stage PFC Converter

OVERVIEW OF PFC

This is because most loads require a supply voltage V2 with low ripple, which is obtained by using a correspondingly large capacitance of the output capacitor Cf . Consequently, the conduction intervals of the rectifier diodes are short and the line current consists of narrow pulses with an important harmonic content. The simplest way to improve the shape of the line current, without adding additional components, is to use a lower capacitance of the output capacitor Cf . When this is done, the ripple of the output voltage increases and the conduction intervals of the rectifier diodes widen. The shape of the input current becomes also dependent on the type of load that the rectifier is supplying, resistive or constant power, as opposed to the case of negligible output voltage ripple where the type of load does not affect the line current. This solution can be applied if the load accepts a largely pulsating DC supply voltage and it is used, for example, in some handheld tools. The concept is highlighted by the simulated waveforms shown in Figure, for two values of the output capacitor and assuming constant power load. The shape of the input current is improved to a certain extent with the lower capacitance, at the expense of increased output voltage ripple, as can be seen also from the results listed in the caption.

We would like to clarify here that, throughout this study, the purity factor Kp , the displacement factor cosφ and the power factor PF , are given only as basic information on the PFC properties of the simulated circuits, and they are not relevant as such for assessing compliance with standard IEC 1000-3-2.

The method presented above has severe limitations: it does not reduce substantially the harmonic currents and the output voltage ripple is large, which is not acceptable in most of the cases. Several other methods to reduce the harmonic content of the line current in single-phase systems exist, and an overview of the representative ones is presented next.

EXTENSION TO OTHER PFC TOPOLOGIES

Although boost PFC's are the most diffused, other converters like flyback, Cuk and Sepic are well suited for PFC applications. All of these overcome some of the problems encountered with the boost topology: for example, they allow high-frequency insulation, voltage step-up and step-down as well as start-up and overload protection. For these converters, some of the above control techniques have been proposed, with proper modifications to suit the different topology characteristics. We will first analyze the flyback PFC, which is the simplest solution for isolated converters, and then Cuk and Sepic structures.

Flyback PFC - The first control strategy proposed for this converter was the Discontinuous current PWM control. According to this technique, the converter draws a sinusoidal current with no need of duty-cycle modulation, i.e. at constant on-time and switching frequency. This very simple approach is convenient for low-power applications, while for medium power levels it is better to operate the converter in continuous conduction mode (CCM), thus reducing the current stresses in the switch.

Cuk and Sepic PFC - These topologies are less popular as PFC due to their higher complexity as compared to boost or flyback structures. Like the flyback converter, they draw a sinusoidal input current, when working in DCM, with no need of duty-cycle modulation. In this case the simple discontinuous current PWM control can be profitably applied. With these converters, however, input current can be continuous even in DCM, which happens when the freewheeling diode current, which is the sum of the two inductor currents, zeroes. With a proper choice of the two inducance values, the input inductor current can be continuous even if the diode current is discontinuous.

THE NEED FOR PFC

Many techniques and topologies can and have been deployed for PFC. Numerous articles have been published that survey the options available for both passive and active PFC. A detailed discussion of the full breadth of options, architecture and topologies would be beyond the scope of this topic, but some of the most commonly used approaches are briefly mentioned here. To meet only the requirements of EN61000- 3-2, very low THD and unity PF are not required. Therefore, at low power levels (up to maybe 200 W), various passive PFC techniques have been employed to spread the conduction angle of the current waveform.

Although passive PFC can be low cost and easy to add to existing noncompliant designs (literally as a “bolt-on” fix) to meet EN61000-3-2, it does add considerable size and weight, degrades overall efficiency, and is limited in the extent of achievable PF improvement. A design that meets EN61000- 3-2 with a 10% margin on all harmonics could have a PF as low as 0.76. Recent ENERGY STAR specs also now require a minimum PF of 0.9 at full load and 115 V/60 Hz. So a design that just about passes the requirements of EN61000-3-2 may not meet ENERGY STAR requirements. On the other hand, as cited in Reference, a PF of 0.9 could be achieved by drawing a square-input current waveform, but such a current waveform could not meet EN61000-3-2 because all harmonics above the 11th would exceed the limits.

CONCLUSION

The comparative study of the buck, boost and interleaved boost topologies for active power factor correction in AC-DC converters has been carried out in this paper. The performance parameters for various active power factor corrected power converter topologies have been tabulated and compared. From the results, it is found that the Interleaved Boost Converter topology for Active power factor correction is the best among the three topologies as it affords improved Total Harmonic Distortion and power factor closer to unity. The power factor can be corrected still more by adopting a closed loop current control strategy such as Average current control, Peak current control, Hysteresis control or Borderline control.

After that, we extended our research by examining two-switch fourth-order topologies, the aim being to explore the possibility of realizing a PFC stage having an input current with reduced high-frequency content, inherent PFC property and an output voltage lower than the amplitude of the sinusoidal input voltage.

From the discussions in this report, it is clear that the power factor correction is being given considerable importance for low and medium power applications. Also seeing that power electronic equipments are increasingly being used, they pretense a serious problem of lower order harmonics on utility side. Among various schemes available for PFC(power factor control), the single stage scheme is preeminent for low and medium power application because of its cost effectiveness, small component size. But in this scheme, there is a serious limitation of high dc link voltage rise under light load condition. This problem can be addressed by using the concept of Parallel Power Flow. In this paper, several control techniques specifically developed for PFC boost converters are analyzed. For each control strategy advantages and drawbacks are highlighted and information on available commercial IC's is given. Extension of these control techniques to other PFC topologies are discussed and some experimental results based on a PFC Sepic converter with different control methods are reported.

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