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RF Interconnects and Embedded Passive Component Modeling In RF System in Package

Kantharao Boggarapu Mallaiah[1]* Dr. Rakesh Kumar[2]

[1]Research Scholar

Abstract – The Packaging Research Center has been creating cutting edge system on-a package (SOP) technology with RF Interconnects, and optical system combination on a single package. SOP aims to use the best of on chip SOC coordination and bundle reconciliation to accomplish most astounding system performance at the lowest cost. The microminiaturized multifunctional SOP package is exceptionally incorporated and manufactured on extensive range substrates like the wafer to-IC concept. Notwithstanding novel blended signal design techniques, SOP research at PRC is focused at creating enabling technologies for bundle level coordination including ultra-high thickness wiring, embedded passive components, embedded optical interconnects, wafer level bundling and fine pitch gathering. A few of these enabling technologies have been as of late coordinated into the main successful system level showing of SOP technology utilizing the Intelligent Network Communicator (INC) test bed. This paper gives an account of the most recent INC and SOP test bed comes about at the PRC and gives knowledge into the future SOP incorporation procedure for merged microsystems. The concentrate of this paper is on incorporation of materials, procedures and structures in a single package substrate for System on-a Package (SOP) implementation.

Keywords: RF Interconnects, Embedded, Passive, Component, Modeling, RF System, Package, Research Center, Developing, SOP, Achieve, Performance, Technologies, Network.

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INTRODUCTION

The Packaging Research Center has been creating System on a bundle (SOP) technology as a superior, minimal effort answer for convergent Microsystems (Fillion et. al., 2005). The essential approach to SOP is the coordination of components and works in the bundle prompting higher performance, smaller, more dependable full framework modules at lower cost. Various SOP building block technologies have been shown at the PRC and fractional coordination of advanced and RF functionality at the bundle level has been accounted for in the past few years (Palm et. al., 2004, Chiriac et. al., 2008). A number of SOP technologies have as of late been incorporated into a blended flag broadband communication model called the Intelligent Network Communicator (INC). The INC test bed incorporates computerized, RF and optical usefulness in a single package created on expansive zone natural substrates using low cost processes. This paper examines a portion of the current developments in component integration and scaling down of advanced, RF and optical SOP substrates and modules at the PRC. INC system architecture, design and electrical test outcomes are being accounted for somewhere else (Pucha et. al., 2001). and this paper covers the combination of packaging technologies with particular concentrate on materials, forms, and reliability.

REVIEW OF LITERATURE:

Technologies for the embedding of dynamic and passive components into develop layers of substrates have pulled in expanding consideration amid recent years. Different embedding technologies have been created because of different requirements concerning electrical performance, chip dimensions, and interconnection (Fillion et. al., 2005, Palm et. al., 2004, Chiriac et. al., 2008, Pucha et. al., 2001). Some of those technologies are now develop enough for increase in expansive scale generation in the mobile communication sector. Fraunhofer IZM and TU Berlin together are creating innovations for embedding of active chips and inactive parts for SOP applications. The primary improvement was the supposed Chip in Polymer technology, which permits acknowledgment of SIPs and in addition sheets with integrated components (Windlass et. al., 2001). In the EU financed extend HIDING DIES industrial and scholarly accomplices combined their skill and accomplished a stable technology platform for highest integration. The embedding technology has utilized effectively overlay of RCC and laser by means of interconnects to chip pads. At PCB

manufacturing level, 50 µm thin chips have been embedded with contributes down to 200 µm up to 18"x24" boards. At model level, embedding of chips down to 100 µm pitch was figured it out. Imaginative strategies for embedding of thick chips have been exhibited by utilizing prepregs in mix with RCC. The HIDING DIES extend has effectively demonstrated the enormous mechanical capacities of chip embedding for scaled down electronic systems and hence has started gigantic intrigue for industrial selection. Inside the HIDINGDIES project, the bland technology was additionally created to offer adaptable answers for the acknowledgment of 3D-SiPmodules.As a successor of HIDING DIES, the new EU-supported venture "HERMES" has introduced with wide investment of Indian industries and research institutes with a more extensive extent of assisting the embedding technology outskirts at R&D level and all the more imperatively of acquiring embedding technology genuine assembling PCB production (Davis et. al., 2001). This paper will give an outline about the Chip in Polymer embedding technology and presents the new challenges and ideas on R&D level to conquer the rising fine pitch requests. Moreover acknowledged applications will be exhibited, concentrating on bundle acknowledgment and RF modules (Fuhan et. al., 2004). The technical and industrial issues related with industrialization of embedding technologies will be declared quickly.

RF IN A SINGLE PACKAGE:

The concept of System-On-Package (SOP) can be thought of an applied worldview in which the package, and not the massive board as the framework and the package provides all the framework capacities in one single module, not as a collection of discrete parts to be associated together, yet as a persistent converging of different coordinated thin film technologies to include a system solution in a small package. This is expert by co-outline and manufacture of computerized, optical, RF and sensor functions in both IC and the package, in this manner advancing capacities that are proficient best at IC level and at package level. A case of a development SOP package with combination of three functions is shown in Figure 1.

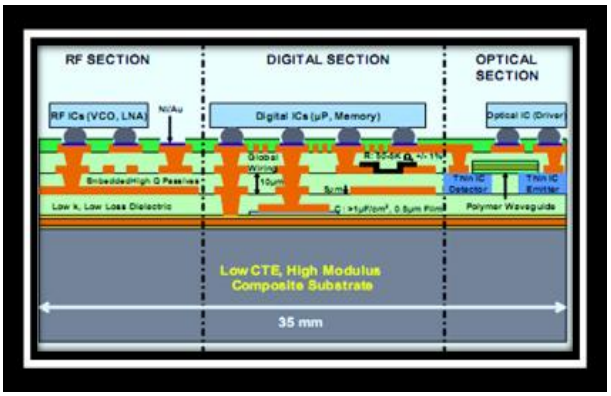

Figure 1: RF section, Digital section and Optical section in a Single Package

RF INTEGRATION:

The SOP also permits productive coordination of finish uninvolved RF front-end useful building blocks, for example, channels and power combiners. Late advancement of thin film RF materials and processes makes it conceivable to incorporate RF front finishes proficiently in the bundle to meet stringent wireless communication needs (Tummala et. al. (2002). A few low misfortune and low k polymers including epoxy, A-PPE, Avatrel, BCB, polyimide, and LCP have been assessed for signal speed and misfortune at GHz frequencies. The ordinary electrical properties of these materials are shown in Table 1.

Table 1: Properties of Low Loss Polymers at 1GHz

Thin/Thick Film Dielectric	ε	Tan δ
Polyphenyl Ether (A-PPE)	3.2	0. 005
Liquid Crystal Polymer (LCP)	2.9	<0. 003
Polyimide	3.3-3.5	0. 005
Polynorbornene (Avatrel^{TM})	2.5	<0. 001
Benzocyclobutene (BCB)	2.7	0. 0008

Multilayer develop wiring has been utilized to incorporate the parts found in RF front closes. The 3D design approach utilizing multi-layer topologies prompts high quality components for multi-band, more extensive data transfer capacity and multi-gauges in a very compact from factor and low-cost. Embedded inductors with Q factors in abundance of 150 have been accounted for (Liu et. al., 2002).

EMBEDDED FILTERS:

A few embedded filters were designed for the SOP process utilizing epoxy materials for the buildup layers. The band pass filter design for C band applications comprises of a square fix resonator with inset bolster lines, as shown in Figure 2. The inset holes go about as little capacitors and exactness lithography with <5% variety in line widths and spaces empowers info and yield coordinating. Estimation result shows that bandwidth of 1.5 GHz and a base insertion loss of 3 dB at the center frequency of 5.8 GHz

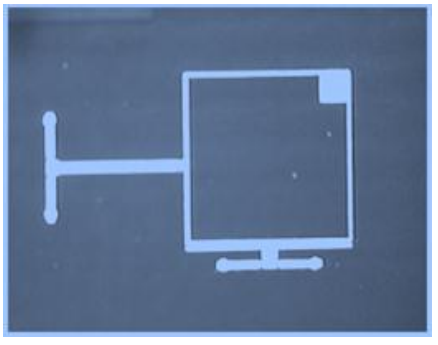

Figure 2- Fabricated Band pass filter for C-Band

EMBEDDED PHOTO DETECTORS:

The waveguides have been integrated with embedded thin film I-MSM and commercial Pin photodiode detectors (Ceramic Matrix 2005). Figure 3 shows an embedded 10 Gbps Pin detector from AXT. The detector IC was first embedded in a thick polymer, followed by cladding and waveguide core fabrication. Contact pads for electrical connection were opened lithographically in the cladding layers. The detector was evanescently coupled to the waveguide and gratings can be used for greater coupling efficiency.

Figure 3- Embedded 10 Gbps Pin detectors in polymer waveguide on FR-4 board

Thin films I-MSM detectors, typically 1 µm thick, with a 20 ps response and a large active area have also been embedded in siloxane and BCB waveguides. The MSM thin film detector was attached to thin film gold pads by thermal treatment (Figure 4) and a waveguide core was formed across the detector.

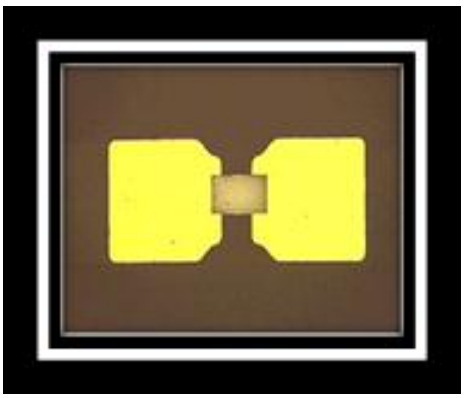

Figure 4- Embedded thin film MSM detector on an FR-4 board prior to waveguide fabrication

INC TEST BED FABRICATION PROCESS:

The INC test bed was designed based on broad plan libraries created in prior years utilizing the PRC standard substrate process technology and the INC-1B card measures 4" x 5". The SOP baseline procedure was produced on 300mm x 300mm boards of high Tg natural overlay utilizing thin film develop miniaturized scale via technology. The substrate materials incorporate Hitachi LX-67 and LX-67F low misfortune overlays, and Nalco N4000-13 high Tg (210°C) covers of 1mm thickness with 1/4oz copper thwart (nominal thickness of 9µm) on each side. The development dielectric utilized was negative photo image capable liquid epoxy, Probelec 81/7081TM. This photograph by means of dielectric has a dielectric consistent of 3.4 and loss of 0.015 at 1 GHz. The development structure comprised of three metal layers with two staggered photo via layers. Embedded capacitors were manufactured utilizing a 10µm thick layer of epoxy-BaTiO3 Nano composites with capacitance density of 10-15nF/cm2. After the electrical wiring fabrication, photo imaginable polymer waveguides were turn covered and lithographically characterized to 50 micron widths. The optical waveguide handle comprised of up to seven different layers including planarization, claddings and the core waveguide. The waveguide terminations were end cleaned to accomplish good coupling proficiency from outside optical fibers. The poly siloxane was chosen in view of a cure temperature of 160°C, underneath the most extreme utilize temperature of both the center cover and the development epoxy dielectric. The standard procedures of the procedure included 25µm lines and spaces, 75-100µm small scale vias, 10µm thick copper metallization, 30µm dielectric thickness, and 3-8µm thick optical layers. The sheets were done with a layer of Taiyo AUS-5 liquid photo imaginable solder cover (15µm thickness) and cushion complete utilized was electro less nickel, drenching gold for get together of SMT components. Figure 5 demonstrates a created INC-1A substrate and delineates agent cross-areas of digital, RF and optical blocks.

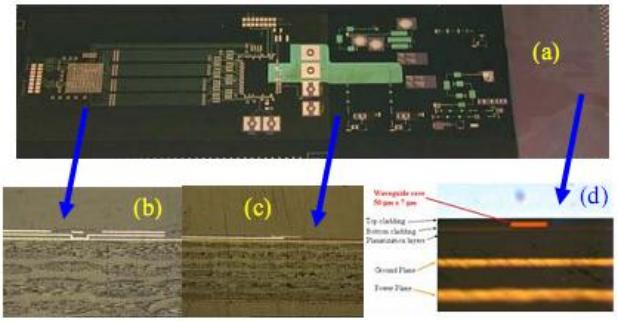

Figure 5- (a) Top View of Fabricated INC-1A Substrate and Cross-sections of (b) Digital Block, (c) RF Combiner, and (c) Optical Waveguides Integrated in INC Module

After introductory substrates were created and tested, additional substrates were co-created with Endicott

Interconnect (EI, previous IBM Endicott) for reliability testing.

INC ASSEMBLY PROCESS:

Digital components including FPGAs, MUX and transceiver chips were then collected in BGA arrangement and some high value latent segments were likewise gathered utilizing sans lead patch. The chip attaches additionally included wire holding for VCOs in the RF section. The input and outputs for the Digital and RF signal are through edge associates. The board is reflowed after screen printing patch glue and gathering utilizing a profile having a greatest temperature of 190°C. Care is taken to improve the profile and the temperature increase is <20C/min to anticipate war page of the multi-layered substrate. Figure 6 demonstrates the best perspective of an assembled INC-1B module.

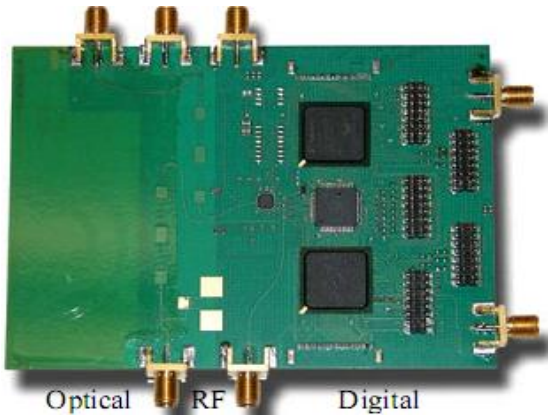

Figure 6- Assembled INC-1B Module with Embedded RF Components and Optical Waveguides

CONCLUSION:

A few empowering technologies for SOP with digital, RF and optical incorporation in a solitary, microminiaturized package have been created. Some of these technologies, including high-density interconnect; embedded passives, embedded RF components, and embedded optical waveguides have been coordinated into the primary exhibition of SOP module utilizing the INC test bed. Future plans for SOP integration incorporate ultra-high thickness wiring to help 50-100µm pitch flip chip utilizing low misfortune dielectrics like BCB; high k, thin film capacitors with >1µF/cm2 capacitance density; and embedded lasers and photo detectors for optical chip to chip interconnects. In the outcome for the chip embedding technology, the semiconductor chips are fully embedded into a level bundle, which can be taken care of like a standard SMD component at that point. The adjustments in the process chain are a colossal challenge for a customary PCB manufacturer. To confront this challenge and to advance towards industrialization, the new project will concentrate mostly on industrial adjustment of embedding technologies.

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Corresponding Author

Kantharao Boggarapu Mallaiah*

Research Scholar

E-Mail –