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An Efficient N Bit Multiplier Design Based on Vedic Mathematics

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Abstract – In this paper, a high speed N bit multiplier based on Vedic mathematics "Urdhva Tiryakbhyam" is proposed. in order to decrease the delay and power consumption in the processing of the signals in the system. The most significant aspect of the proposed method is that, the multiplier design is based on vertical and crosswise structure of Ancient Indian Vedic Mathematics .It generates all partial products and their sum in one step. The delay of proposed multiplier is compared with Array multiplier. The synthesis results show that, the N bit multiplier based on Vedic mathematics "Urdhva Tiryakbhyam" has a less delay compared to the array multiplier. The results indicates that the N bit multiplier based on Vedic mathematics " Urdhva Tiryakbhyam" has great impact on improving the speed of signals in the field of signal and image processing.

Keywords: Vedic Mathematics, Urdhva Tiryakbhyam, Sutra, VHDL, Multiplier.

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INTRODUCTION

The field of digital signal processing and image processing has grown as an important field of study both theoretically and technologically. The multiplication is an important fundamental function in arithmetic operations. The complex multiplication is an essential requirement in the field of signal and image processing**.** The paper is organized as follows. Section II describes the basic methodology of Vedic multiplication techniques. Section III describes the architecture of conventional multiplier techniques. Section IV describes the proposed Vedic multiplier design. Section V describes the results. Finally section VI comprises of conclusion.

II. VEDIC MULTIPLICATION METHOD

Vedic mathematics is mainly based on 16 Sutras (or aphorisms) dealing with various branches of mathematics like arithmetic, algebra, geometry etc. In this paper, the designed multiplier is based on Urdhva Tiryagbhyam sutras which means vertically and crosswise. The partial products and their summation of multiplication are obtained parallel in Urdhva Tiryagbhyam multiplier.

These sutras have been traditionally used for multiplication of two numbers in decimal number system. The following example shown below illustrates decimal multiplication using Urdhva Tiryakbhyam**.**

4 4 ⇓

3 2

: 8

4 4 ⤫

3 2

8+12 : 8

4 ⇓ 4

3 2

12+2 : 0 : 8

Result = 44 X 32 =1408

III THE ARCHITECTURE OF CONVENTIONAL MULTIPLIER

Consider two four bit binary numbers A and B multiplication.

				A3	A2	A1	A0
				B3	B2	B1	B0
				A3B0	A2B0	A1B0	A0B0
			A3B1	A2B1	A1B1	A0B1	
		A3B2	A2B2	A1B2	A0B2		
	A3B3	A2B3	A1B3	A0B3			
P7	P6	P5	P4	P3	P2	P1	P0

To implement this multiplier we require twelve 3 input, 2 output adders. This parallel multiplier is known as Braun multiplier and this is the basis for most of the today's commercial application.

IV. THE PROPOSED VEDIC MULTIPLIER DESIGN

Consider two four bit numbers denoted as n1H n1L and n2H n2L, where n1H and n2H corresponds to the most significant bits; n1L and n2L are least significant bits. When the numbers are multiplied according to the Urdhva Tiryakbhyam method, we get

n1H n1L

X

n2H n2l

=

(n1H x n2H) + (n1H x n2L + n2H x n1L) +

(n1L x n2L) (1)

Thus , from the above equation (1) we need:-

Four 2 bit multiplier and three 4 bit ripple carry adder.

To implement proposed 8 bit multiplier we required

four 4 bit multiplier and three 8 bit ripple carry adder.

The following example shown below illustrates binary

multiplication using Urdhva Tiryakbhyam sutras.

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A= 1 0 1 1

B= 1 1 0 1

First multiplication of AL and BL

1 1

0 1

: 1 1

1 1

0 1

---

1 0 1

1 1

0 1

---

i. 0

Result= AL x BL = 011------(2)

Next multiplication of AH and BL and AL X BH

1 0

0 1

: 0 0

1 0

0 1

---

0 1 1

1 0

0 1

---

0 0

Result= AH x BL =010 ----- (3)

AL x BH

1 1 ⇓

1 1

: 1 1

1 1 ✕

1 1

---

1 1 0 0

1 ⇓ 1

1 1

---

1 1

Result= AL x BH =1001 -----(4)

Result= (AH x BL) + (AL x BH) = 1011 ------- (5)

finally multiplication of AH and BH

1 0 ⇓

1 1

:0 0

1 0 ✕

1 1

---

1 0 1

1 ⇓ 0

1 1

---

1 1

Result= AH x BH = 110 ------- (6)

Finally if the number is (4 x 4) bit shift the result by two. For (8 x 8) bit shift result by four and so on.From equations 2, 5, and 6 we get

AL x BL = 011

(AH x BL) + (AL x BH)= 1011

AH x BH = 110

Result= A x B 10001111 ----- (7)

The architecture of Vedic Multiplier

	A3			A2		A1		A0
	B3			B2		B1		B0
P8	P7	P6	P5	P4	P3	P2	P1	P0

V. SIMULATION RESULTS

The proposed method was implemented using VHDL and logic simulation was done using Xilinx ISE simulator. The synthesis was done using Xilinx project navigator. The design was synthesized for Spartan3(xc3s200-5-ft256)device.

The following table I shows the simulation Results comparison.

Table I : simulation results :

	8 bit Array Multiplier	**Proposed Vedic Multiplier**
No. of slices utilized	95	53
No. of 4 i/p LUTS utilized	165	94
No, of bonded IOBs utilized	32	32
Delay	34	13

VI. CONCLUSION

The advantage of proposed architecture based on vedic mathematics compared to parallel multiplier is that less resources are required such as multipliers

and adders. The results show that the N bit multiplier based on vedic mathematics is more faster than the conventional multiplier.

In future, the other sutras of vedic mathematics can be applied in different domain of engineering and the other fields.

REFERENCES

L. Ciminiera and A. Valenzano, “Low Cost Serial Multiplier for High Speed Specialised Processors”, IEE Proc., vol. 135, no. 5, pp. 259– 265, Sept. 1988.

Wey C.L. and chang T.Y., “ Design and analysis of VLSI Based Parallel Multiplier,” IEEE Proc. 1990,137,(4), pp. 328-336.

S. He, and M. Torkelson, "A pipelined bit serial complex multiplier using distributed arithmetic," in proceedings *IEEE International Symposium on Circuits and Systems*, Seattle, WA, April 30 -May- 03,1995,pp. 2313-2316

Prabir Saha et.al. “A High speed ASIC design of complex Multiplier using vedic Mathematics,” in proceedings of the *2011 IEEE student Technology Symposium*, 14-10 January 2011,IIT, Kharagpur.

Zhijun Huang, Milos D. Ercegovac, "High-Performance Left to Right Array Multiplier Design," arith, pp.4, 16th IEEE Symposium on Computer Arithmetic (ARITH-16 '03),2003.

Jung -Yup Kang and Jean-Luc Gaudiot , “ A Simple High - Speed Multiplier Design,” IEEE trans. on computers, vol. 55, no. 10, pp. 1253-1258,October 2006.

L. Ciminiera and A. Valenzano, “Low Cost Serial Multiplier for High Speed Specialised Processors”, IEE Proc., vol. 135, no. 5, pp. 259– 265, Sept. 1988.

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