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Design and Implementation of Low Power CMOS Flash ADC in Cadence Tool

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Abstract – Analog to digital converter is a critical device, has huge applications in today's digital world. This paper describes the design of FLASH ADC using 180nm CMOS technology. The FLASH has highest speed among all the other ADCs due to its parallelism. This consists of series of comparators which give thermometer coded outputs which is converted to the digital form by an encoder. The main disadvantage of this ADC is its power consumption. Comparators are the power hungry circuits whose power dissipation is reduced. The main aim of this paper is to design low power FLASH type ADC. Pre-layout and post layout simulation is done using cadence virtuoso analog design environment. The comparators output is encoded using an encoder designed with full adders to reduce the number of transistors.

Keywords—Analog to Digital Converter, Full Adder Comparator, Thermometer Code, Encoder.

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INTRODUCTION

The signals in the real world are analog in nature, for example light, sound, video etc. Since digital circuits are more robust, transmission errors are less, offer greater advantages over analog circuits in processing speed and are more efficient. Hence it is always better to process and transmit the information in digital form and finally it can be converted to analog form. So, in order to obtain digital signal, we need to make use of Analog-to-Digital converters and whenever, we need the analog signal back then digital-to analog converters are required. The data converter applications range from audio communication to medical field. These converters are implemented using a variety of architectures. The ADC is characterized by three factors namely speed, area and power consumption. The flash ADC is the fastest one among all ADCs because of its parallel operation. This is suitable for applications requiring very large bandwidths. This paper presents systematic design of 3-bit flash ADC implemented in 180nm CMOS technology. This work includes the design of high speed flash ADC with an encoder with less number of transistors. This paper is organized as follows. Section II describes the system architecture and deals with the design of building blocks. Section III briefly covers simulation results.

II. SYSTEM ARCHITECTURE

Figure1 shows the typical flash ADC [1] block diagram. It has resistive a ladder network to generate the internal reference voltages for the comparators. The number of resistors is 2^N and comparators required are 2^N -1 for N bit ADC. The comparators output is thermometer code which is converted to the digital form by an encoder designed with full adder circuits.

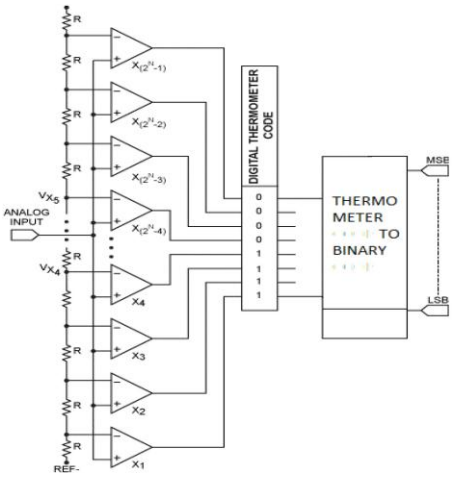

Figure 1. Block diagram of Flash ADC

A. Reference Generator

The reference voltages are generated with a resistor ladder in which each resistance is of same value. For n bit converter 2^N are required. We have used poly resistors to build the resistor array. The resistor value is calculated by,

$$V_{LSB} = (Vref_+ - Vref-)/ 2^N \qquad (1)$$

The V_{LSB} indicates the difference between adjacent reference voltages. Which have to be applied to the comparator arrary.

B. Design of Comparator

Comparator is critical part of the ADC design. Here we use two staged op amp in designing the comparator circuit. Below Figure 2 shows the structure of two stage op amp comparator.

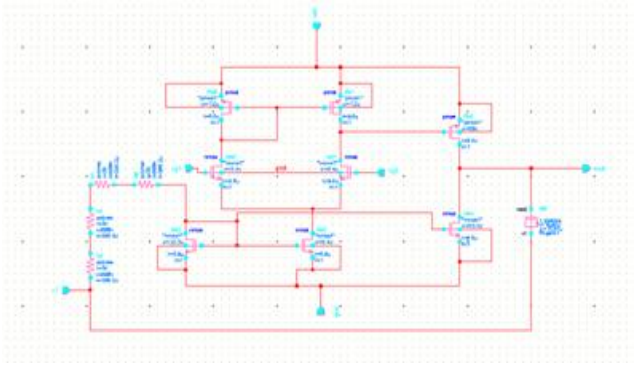

Figure 2. Schematic of two stage comparator

First stage is a differential amplifier to reduce the noise and second stage is common source amplifier to have higher gain. The biasing technique is of current mirror type.

C. Design of Encoder

Encoder is the digital part of the ADC which converts thermometer coded input signal to the normal digital output. For 3-bit FADC the thermometer code is of 7 bit, the outputs of the comparators as indicated in below table.

Table I :Truth table of Thermometer to binary encoder[2].

Thermometer code							Binary code		
C7	C6	C5	C4	C3	C2	C1	B3	B2	B1
0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	0	0	1
0	0	0	0	0	1	1	0	1	0
0	0	0	0	1	1	1	0	1	1
0	0	0	1	1	1	1	1	0	0
0	0	1	1	1	1	1	1	0	1
0	1	1	1	1	1	1	1	1	0
1	1	1	1	1	1	1	1	1	1

In this paper the encoder circuit is designed using cascading of full adders. Each of the adder schematic uses 10 Transistors. This circuit is designed using XOR and XNOR logic.

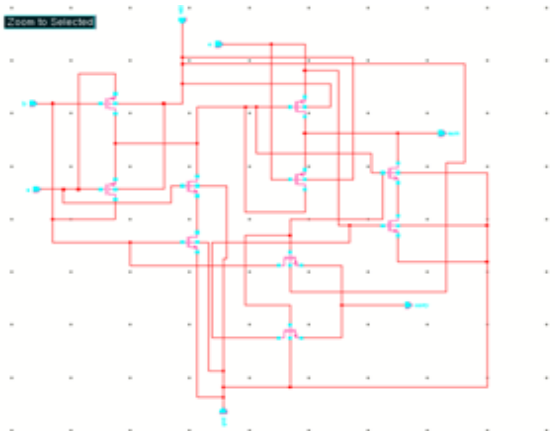

Figure 3. Full Adder circuit

For the designed 3-bit ADC we need four full adder circuits and three delay circuits to apply the inputs simultaneously. Figure 4 below the shows the encoder schematic diagram.

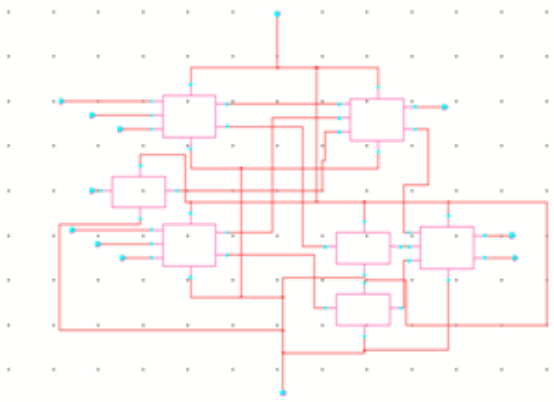

Figure 4. Encoder circuit

Figure 5 shows the block diagram of designed 3-bit flash ADC.

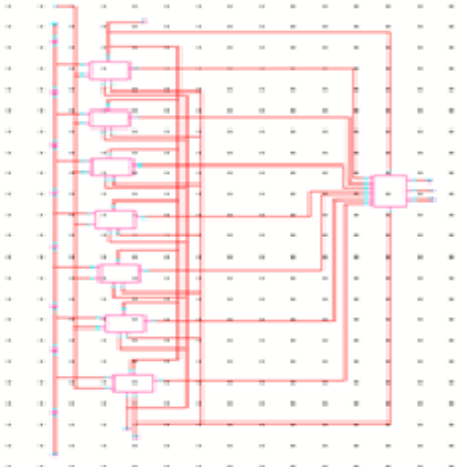

Figure 5. Designed 3-bit FADC

III. SIMULATION RESULTS

The schematic and layout of the designed 3-bit flash ADC are simulated using cadence 180nm technology with Virtuoso analog design environment.

3-bit Flash ADC in 180nm technology using Virtuoso analog environment design of cadence tools. Pre-layout and Post layout simulation results.

A. Pre- layout results

1. Comparator output waveform

As shown in below Figure 6, a sinusoidal wave is applied to the noninverting terminal of the comparator and reference signal is applied to the inverting terminal. The resulting output of the comparator goes high when the input voltage at the noninverting terminal surpasses the reference voltage applied at the inverting terminal.

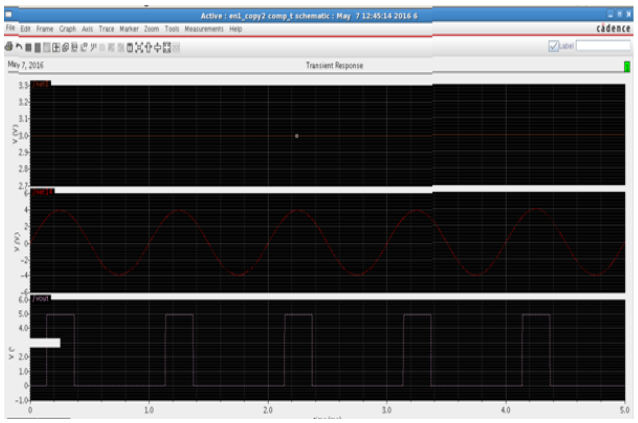

Figure 6. Comparator output

2. Encoder output

As the encoder uses 10T full adders below Figure 7 shows the output of 10T full adder and the Figure 8 represents the output of encoder

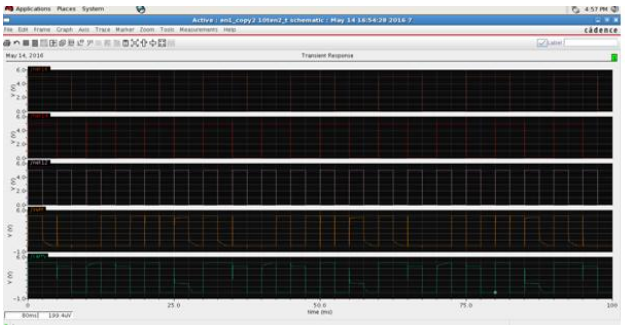

Figure 7. Output of 10 Transistor fulladder

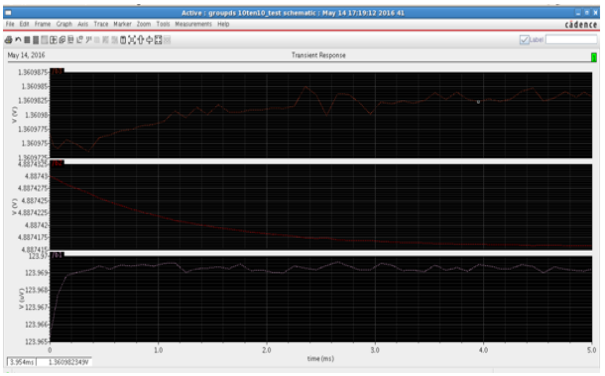

Figure 8. output of the encoder

B. Post layout simulation results

1. Layout of Comparator

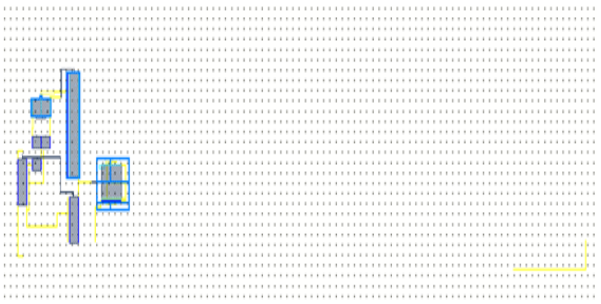

Figure 9. Comparator Layout

2. Layout of the Encoder

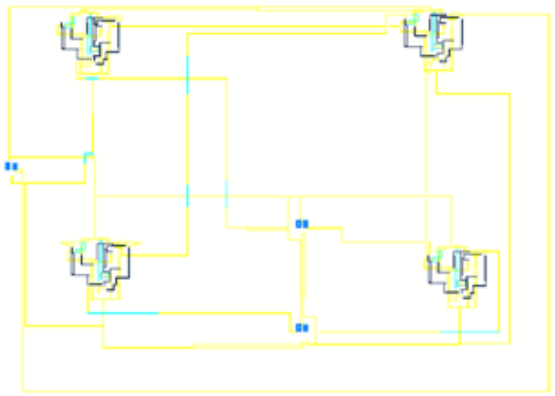

Figure 10. Encoder Layout

3. Layout of ADC

The Figure 11 shows simplified layout of complete 3-bit Flash type ADC. It includes resistive ladder network designed with poly layers, to generate the seven required reference voltages.

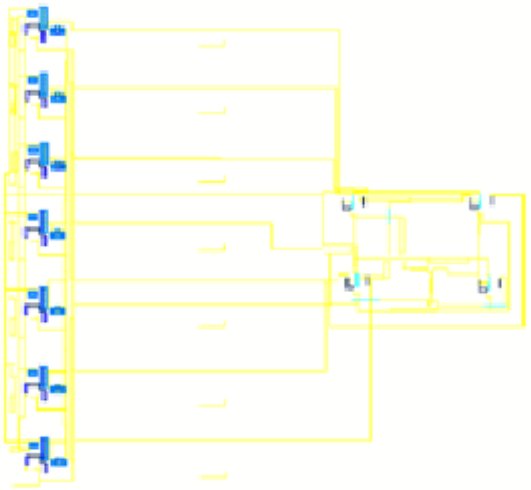

Figure 11. Layout of 3-bit flash ADC

These seven voltages are applied at the inverting terminals of the comparators. The input is applied at the noninverting terminal of all the comparator circuits. Depending upon the applied input voltage the comparators produce “high” or “low” output. The seven comparators output forms the thermometer code, is applied to the full adder circuits in desired fashion to have an encoder operation to get the required digital output

CONCLUSION

This paper presented systematic design of 3-bit Flash ADC. This architecture is simulated in cadence analog design environment using gpdk 180nm technology with power supply of 5V.

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REFERENCES

Yatish Lavaniai, George Tom Varghese and K. K. Mahapatra “An Ultra Low Power Encoder for 5 Bit Flash ADC” pp. 978-1-4673-5301-4/13, 2013 IEEE.

Pradeep Kumar, Amit Kolhe, **“**Design & Implementation of Low Power 3-bit Flash ADC in 0.18µm CMOS” International Journal of Soft Computing and Engineering (IJSCE) ISSN: 2231-2307, Volume-1, Issue 5, November 2011.

Sarojini Mandal, Dr.J.K Das “DESIGN OF 3-BIT LOW POWER FLASH TYPE ADC” International Journal of Advanced Research in Computer Engineering & Technology (IJARCET) Volume 3 Issue 4, April 2014.

Samad Sheikhaei, Shahriar Mirabbasi, and Andre Ivanov, “A 4-Bit 5GS/s Flash A/D Converter in 0.18µm CMOS”, pp. 0-7803-8834-8/05, 2005, IEEE.

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