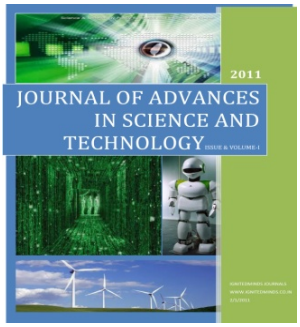

CMOS Comparator for Low Power and High Speed

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Abstract: This paper reports comparator design for low power & high speed. The present Design is specially design for high resolution Sigma Delta Analog to Digital Converters (SDADCs). Design is based on two stage CMOS OP-AMP technique. Simulation results have been obtained by 0.5 micron technology, considering ±2.5 supply voltage & 2.5 V Input range. Design has been carried out in Tanner tool using HP 0.5 micron technology. Simulation results are verified using S-Edit and W-Edit. We have achieved the propagation delay (speed) of 3.6 nano sec. with low power consumption about 0.31 mW. Finally, compare the proposed results with earlier work done [5], [10] and get improvement in presented results.

I Introduction

A comparator is a differential amplifier with no feedback loop, whose function is to compare the analog signals presented at its inputs. Depending on the polarity of the differential input will be the logic output produced. As it is the case with several types of ADCs, usually one of the comparator's input is connected to a constant potential or reference. The circuit symbol and ideal transfer function of a comparator is shown in Figure 1. It can be seen that if the voltage difference Vin + - Vin - is positive the comparator's output will go high (VOH), otherwise its output will go low (VOL).

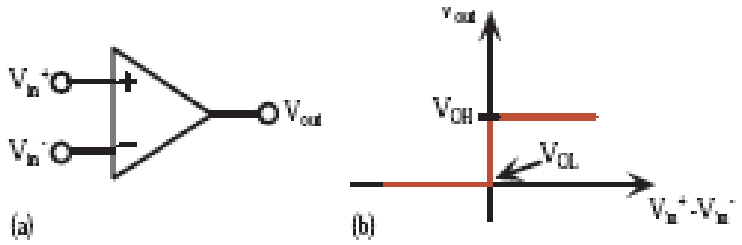

Figure 1. Comparator (a) circuit symbol and (b) ideal transfer function.

1.1 Performance Metrics

Due to fabrication limits and process variations, the comparator performance is affected by nonideal effects. As a result, the response deviates from the ideal one shown in Figure 1(b). Following is a brief description of the main parameters that characterize the performance of comparators.

Static Parameters

The static parameters are those that described the performance of a comparator under DC or steady-state conditions. The main parameters presented here are resolution, gain, offset, noise, and ICMR.

Resolution is the minimum input difference that can be resolved by the comparator in order to switch between its binary states. It is usually limited by the input-referred offset and noise generated by the internal components of the comparator. When employed in ADCs, the resolution specification must be equal or lower than the least-significant-bit (LSB) defined by the converter.

The gain, Av, is one of the key limiting factors in achieving the desired resolution for the comparator. To obtain the ideal response shown in Figure 1, a transition between output logic levels occurs for a zero-input difference. This leads to a gain that approaches infinity, as given by the following equation

A real comparator has a finite gain, given by

$$A_v = \lim_{\Delta V \to 0} \frac{V_{OH} - V_{OL}}{\Delta V} \qquad (3.13)$$

$$A_v = \frac{V_{OH} - V_{OL}}{V_{in}^{+} - V_{in}^{-}} \qquad (3.14)$$

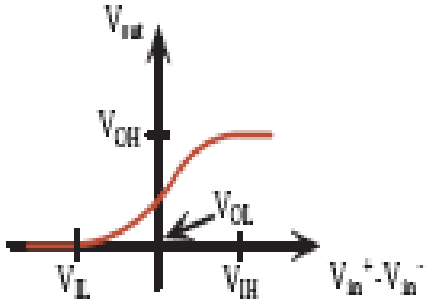

Figure 2. Transfer function of a finite-gain comparator.

As mentioned before, the offset is a non-ideal effect that limits the resolution of the comparator. Assuming an ideal comparator with zero differential input voltage required to produce an output transition, the offset is defined as the minimum amount of input voltage required for the binary-state transition to take place. In a real comparator the offset adds to the minimum voltage for which the resolution was designed reducing the resolution of the circuit. An illustration of how itt affects the response of the circuit is given in Figure 3. Section 3 presents offset-cancellation techniques developed to reduce this kind of error. Noise has great influence on the operation of the comparator, thus affecting the performance of an ADC. From Figure 4, the effect of noise in the circuit's response can be seen as uncertainty in the time when the comparator's output switches between its two states.

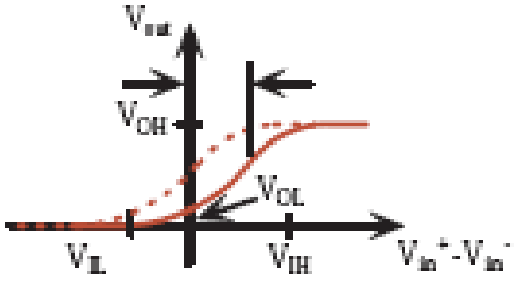

Figure 3. Effect of offset voltage in the transfer function of a comparator.

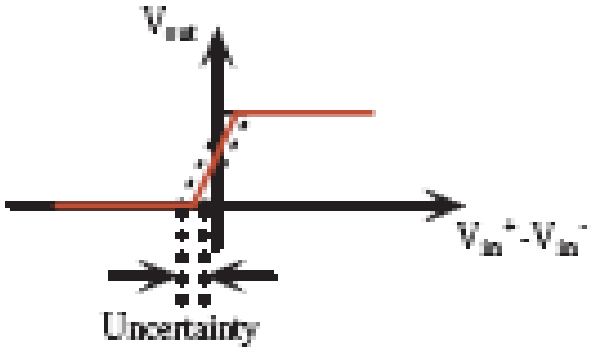

Figure 4. Effect of noise in comparators.

The signal presented to the input of amplifiers and comparators is not fully differential but carries a common-mode component with it. Another important parameter is then the input common-mode range (ICMR). The ICMR is the permissible voltage-range over which the input common-mode signal can vary while all transistors remain biased in the saturation region. If the input signal exceeds this specification, the comparator won't be able to operate properly as some of its transistors could be in triode or cutoff modes.

Dynamic Parameters

Two of the most important dynamic parameters that determine the speed of a comparator are the propagation delay and the settling time. The propagation delay is the time that elapses between an input transition and the corresponding output change. As

shown in Figure 5, it is usually measured at the midpoints between the input and output signals. The settling time, as with a S/H circuit, is defined as the time needed for the output to settled within a specified percent of its final value, usually 0.1 and 0.01%.

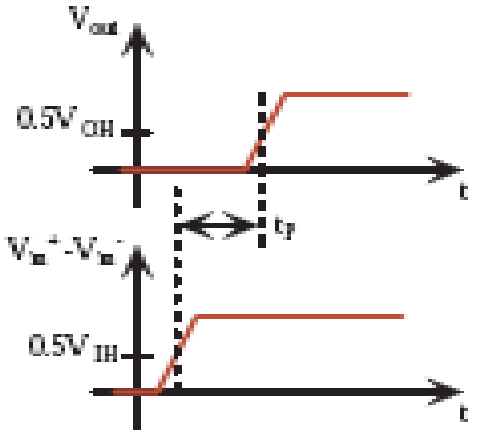

Figure 5. Propagation delay in a comparator.

Figure 6 illustrates the time response of a comparator to a small input signal. It is based on a first-order approximation for an op amp with a single dominant-pole.

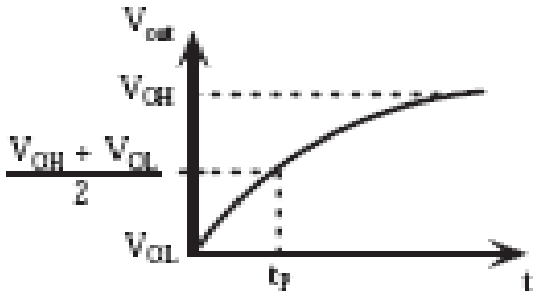

Figure 6. Comparator time response to a small input voltage.

The propagation delay for the time response shown in Figure 6 can be approximated as where p1 is the comparator's dominant pole and tc is its associated time constant.

As with any op amp, the slew rate is a large-signal behavior that sets the maximum rate of output change. It is limited by the output driving capability of the comparator. The propagation delay is inversely proportional to the input voltage applied. This means that applying a larger input voltage will improve the propagation delay, up to the limits set by the slew rate.

II Architecture

Comparators can be roughly classified into open-loop (continuous-time) comparators and regenerative comparators. The main difference resides on whether or not feedback is applied to the op amp used. To obtain the benefits offered by both types of comparators, many configurations have been developed that employ a combination of open-loop stages with regenerative stages that use positive-feedback.

Open-loop Comparators

An open-loop comparator is an operational amplifier designed to operate with its output saturated, close to the supply rails, based on the polarity of the applied differential input. The op amp does not employ the use of feedback and hence no compensation is required to achieve stability in the system. This does not poses a problem since the linear operation is of no interest in comparator design. The main advantage of not compensating the op amp is that it can be designed to obtain the largest possible bandwidth, thereby improving its time response (see equation 3.15).

$$t_p = \frac{1}{p_1}\ln(2) = \tau_c \ln(2) \qquad (3.15)$$

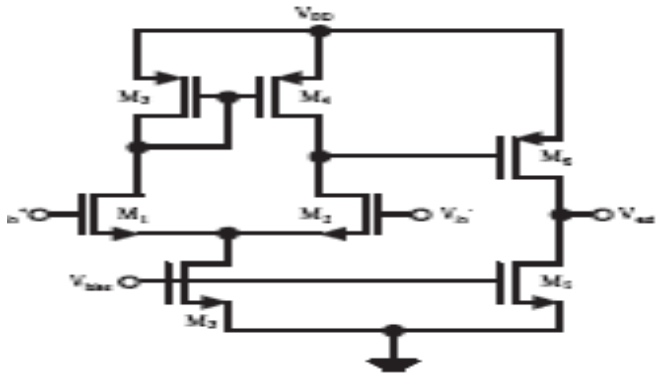

Figure 7. Two-stage open-loop comparator.

Figure 7 illustrates a circuit example of an open-loop comparator. It is based on the commonly used two-stage op amp. The first stage is a NMOS differential-pair consisting of transistors M1 and M2, with PMOS transistors M4 and M5 acting as a diode-connected active load. Transistors M3 is used to bias the input pair. The output stage is a current-sink inverter consisting of transistors M5 and M6.Figure 3.28 illustrates an example of the time response of this comparator.

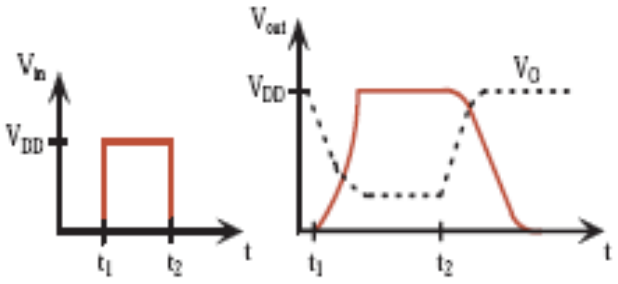

Figure 8. Output response of a two-stage comparator.

The main advantage of open-loop comparators is that, if enough gain is provided, the minimum detectable differential input can be very small (< 1mV). Examining equation (3.14), it would be reasonable to think that by simply designing the comparator with the largest possible gain an almost infinite resolution can be achieved. However, increasing the gain also reduces the bandwidth of op amps. This means that although the

resolution will improve, the time response of the comparator will degrade. Thus, a trade off between speed and resolution must be made. The absolute maximum resolution of open-loop comparators is limited by input-referred noise and the offset voltage present in the op amp used.

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